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Design of DDS Multi-waveform Generator Based on CPLD

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Abstract: Traditional Direct Digital Synthesis (DDS) waveform generators were usually completed by DDS chips, which were expensive and poorly customizable. This paper proposed a CPLD-based DDS multi-waveform generator design. DDS was independently developed and programmed by VHDL language. The system could be interfaced with PC. The system was mainly divided into two parts: upper computer and lower computer. The upper computer part mainly included the main interface design of the system, the sending of control commands and the receiving part of data. The sending and receiving of commands and data was realized by serial communication. The upper computer part was programmed by High-level programming language named DELPHI. The lower computer part mainly included DDS design part, the reception of control commands and the transmission of data, etc., the lower computer part mainly adopt VHDL language to be programmed in CPLD. The DDS design part mainly included the design of the phase accumulator, the design of the ROM, the design of the D/A part, and the design of the low-pass filter. The system could adjust the frequency of the output waveform by adjusting the size of the frequency word, and adjust the waveform shape of the system output by adjusting the internal data of the ROM. Simulation and experimental results showed that: the DDS multi-waveform generator designed by CPLD could achieve the expected goal, and the work effect was good.

Keywords: Waveform Generator, DDS, VHDL, System

1. Introduction

Waveform signal generator was a commonly used signal source, widely used in scientific research, production practice, teaching practice and other fields, such as design and testing, automobile manufacturing, biomedicine, sensor simulation, manufacturing model, etc [1-9]. Waveform generators were mostly composed of oscillators, amplifiers, attenuators, indicators and modulators. The characteristic of this traditional design method was the use of hardware implementation, the hardware connection was complicated, and the reliability was poor. The wide application of hardware description language VHDL and programmable ASIC devices had broken the barrier between hardware and software. Based on the VHDL language, the DDS technology with CPLD as the core had matured, and the related technology had been widely used, and it had also been recognized by experts and scholars at home and abroad. This design was based on CPLD using DDS technology to complete the design of the multi-waveform signal generator, the hardware description language VHDL was used to program the software part of the system, the Delphi language was used to design the PC interface part of the system. Sine wave, triangle wave and other waveform were generated on the experiment plat by DDS technology.

2. DDS Design Principle

2.1. Basic Structure of DDS

As early as 1971, American scholars J. Tierney and C. M. Tader and others first proposed the DDS principle from the perspective of phase. DDS was a direct digital synthesizer, which was a new type of frequency synthesis technology, which had the advantages of relatively large bandwidth, short frequency conversion time, high resolution and good phase continuity. It was easier to realize the numerical control modulation of frequency, phase and amplitude, and was widely used in the communication field. The basic

principle of DDS was based on the Nyquist sampling theorem to realize the control of signal frequency and phase. The basic block diagram of DDS was shown in Figure 1. It was mainly composed of a Accumulator, ROM, a digital-to-analog converter (D/A), and a low-pass smoothing filter.

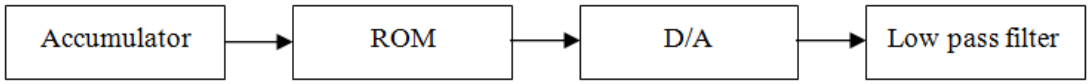

Figure 1. *DDS Basic principle block diagram.*

First, the needed signal waveform would be sampled and quantized to generate data, and then stored them in the memory as a data table of the signal waveform. When outputting the signal waveform, the circuit read out the signal waveform data from the data table in turn under the control of a highly stable clock signal, combined the frequency word and the phase word to accumulate to generate a new digitized signal, which was converted into the desired analog signal waveform by a DAC. The low-pass filter was used to filter out unwanted sampling frequency components and made the frequency spectrum of the output signal pure. The specific structure was shown in Figure 2.

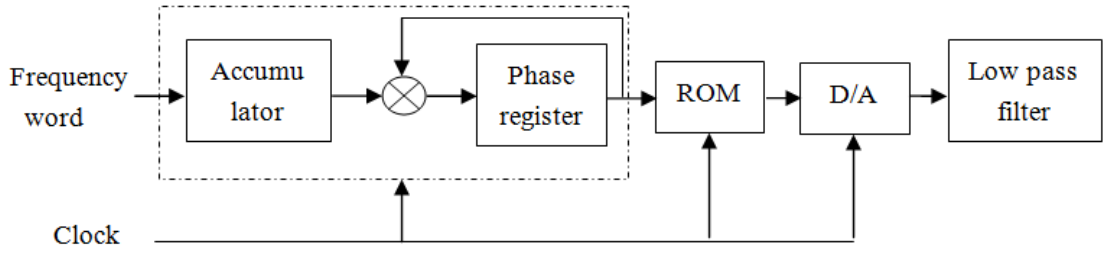

Figure 2. *DDS block diagram.*

2.2. How DDS Works

The core of DDS technology was the phase accumulator. Every time a clock signal came, the output of the phase accumulator increased by a step-length phase increase, and the magnitude of the phase increase was determined by the frequency control word [10-16]. The frequency word (FSW) was actually the phase increment value (binary code) as the accumulated value of the phase accumulator. The frequency control word K was accumulated with the phase accumulator once in each clock cycle, and the phase value obtained was sent to the ROM to look up the table. The output of the ROM was sent to the D/A converter. And the digital waveform amplitude of the form was converted into an analog form signal of the required synthesized frequency. The low-pass filter was used to filter out unwanted sampling components in order to output a pure sine wave signal.

When the frequency synthesizer was working normally, under the control of the standard frequency reference source (the frequency control word determines the corresponding phase increment), the phase accumulator continuously linearly accumulated the phase increment. When the phase accumulator was full, an overflow would occur to complete a periodic action. This action cycle was a frequency cycle of the DDS synthesis signal.

If the number of bits of the phase accumulator was N, the phase increment in the frequency control word was K, and the reference clock frequency was f_C, then:

The frequency f_O of the output signal of the DDS system was:

$$f_O = f_C \times K / 2^N \quad (1)$$

The frequency resolution of the output signal Δf_O is:

$$\Delta f_O = f_C / 2^N \quad (2)$$

Therefore, when the required frequency was input, it would be converted into a frequency control word by the above formula to drive the FPGA to work, thereby generating the frequency of the required waveform.

3. System Software Design

3.1. General Structure Introduction

DDS waveform signal generator design could be divided into the following parts: (1) PC control part; (2) CPLD access data and direct digital frequency synthesis part; (3) D/A conversion part; (4) LPF filter part. Specific design drawing was shown in Figure 3. The direct digital frequency synthesis part was the core part of the entire system. The generated digital signal was converted into an analog waveform through the integrated D/A converter inside the chip, and then smoothed by a low-pass filter to generate the required various Kind of signal.

3.2. PC Part

3.2.1. Interface Design Part

The PC control part was mainly realized by the high-level language Delphi programming, and the design interface was shown as figure 4.

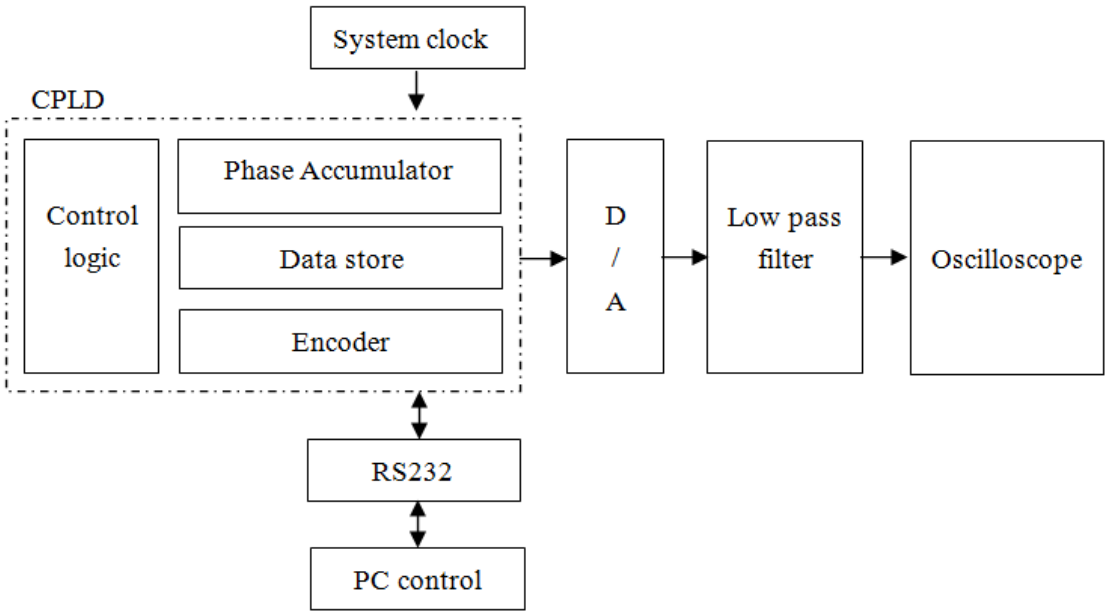

Figure 3. *Block diagram of the overall system design structure.*

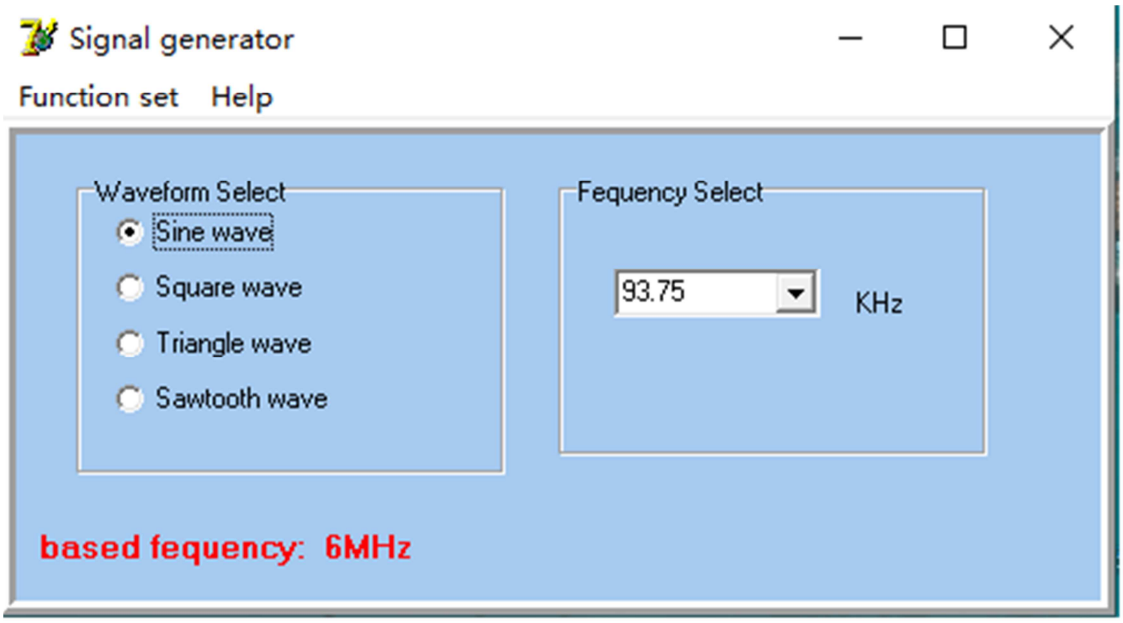

Figure 4. *PC design interface.*

3.2.2. Subroutine Design

The system adopted the serial communication control TCOMM, which was easy to use. Firstly, the serial port would be initialized. After the "OK" key was pressed, the waveform and frequency would be encoded and combined into one byte of data (the upper 4 bits represent the waveform, the lower 4 bits Represents frequency), which would be sent through the serial port. The program design was shown as follows:

```
form1.Comm1.PortOpen:=true; // open the serial port
if form1.RadioButton2.Checked=true then begin
//sine Wave
if form1.ComboBox1.ItemIndex=0 then send[0]:=$01
// frequency 93.75Hz
else if form1.ComboBox1.ItemIndex=1 then send[0]:=$02
// frequency 187.5Hz
…
else send[0]:=$09; // frequency 843.75Hz
end
else if form1.RadioButton1.Checked=true then begin
// Square Wave
…
end
else if form1.RadioButton4.Checked=true then begin
// Triangle wave
…
```

```
end
else if form1.RadioButton3.Checked=true then begin
// Sawtooth wave
…
end;
form1.Comm1.OutputByte(send[0]);
// send command
```

3.3. CPLD Part Software Design

3.3.1. The Overall Design Principle Was Shown as Figure 5

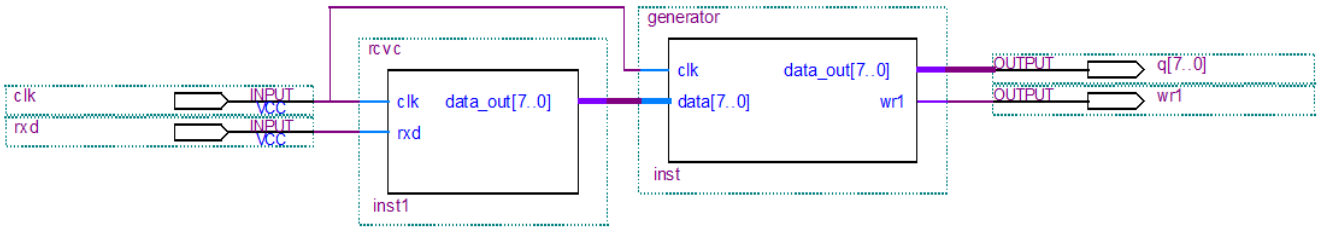

Figure 5. *The overall design principle.*

3.3.2. Phase Accumulation Module Design

This part mainly completed the phase accumulation function, the design procedure was shown as follows.

```
process (REG_Q, A)
begin
TEMP <= REG + A;
-- Phase accumulation
end process;
process(CLK, CLR)
begin
if CLR = '1' then
REG <= "000000";
-- System data reset
elsif rising_edge(CLK) then
if CE = '1' then
REG <= TEMP;
-- Latch output
end if;
end if;
end process;
Q <= REG_Q;
```

3.3.3. Register Module Design

This part mainly completed the latching of addresses and data. Taking 6-bit address latching as an example, the design procedure was shown as follows.

```
process (CLK, CLR)
begin
if CLR = '1' then
TEMP_Q_0 <= (others => '0');
-- System data reset
elsif rising_edge(CLK) then
if CE = '1' then
TEMP_Q_0 <= DATA;
-- Latch output
end if;
end if;
end process;
Q <= TEMP_Q_0;
```

3.3.4. Waveform Selection Module Design

This part used a typical CASE statement to decode, and the program design was shown as follows.

```
case bx is
when "00"=>
-- sine waveform
… -- Output sine wave data
when "01"=>
-- Square Wave
… -- Output square wave data
when "10"=>
… -- Output triangle wave data
when others=>
… -- Output sawtooth data
end case;
```

3.3.5. Design of Receiving Part of Serial Communication Module

The essence of serial communication was to receive data bit by bit under the action of the baud rate generator through the serial port, and then converted it into parallel data output. The core part of the design procedure was shown as follows.

```
if clk1x'event and clk1x = '0' then
std_logic_vector(no_bits_rcvd)>="0000"and
std_logic_vector(no_bits_rcvd) <= "1000" then
rsr(7 downto 1) <= rsr(6 downto 0);
rsr(0) <= rxd2;
elsif std_logic_vector(no_bits_rcvd) = "1001" then
rbr <= rsr;
end if;
end if;
// Convert serial data into parallel data.
```

3.3.6. System Simulation

Taking a sine wave as an example, we had carried out a system simulation on the waveform, and the output was a sine wave simulation waveform as shown in the Figure 6. It could be seen from the figure that the change law of the output data ws a stable sine law.

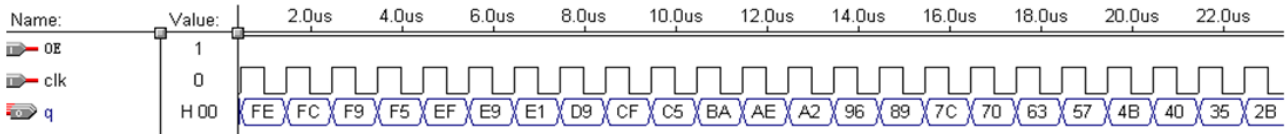

Figure 6. *Sine wave simulation diagram.*

4. Conclusion

Through actual on-site debugging, the system functions were all realized, the signal output was stable. The signal waveform and frequency of DDS could be adjusted by PC, and the output waveform frequency had high precision, and the control interface was humanized, which had strong practical value.

References

[1] Wang Zhen-yu, Wu Xiao-sheng, Shu Sheng-zhu. Research on Precise Signal Generation System of DDS and AGC Controlled by FPGA [J]. Instrument Technique and Sensor, 2019 (1): 55–58+63.

[2] Li Mengting, Li Huafeng. Design of SPWM Wave drive circuit based on DDS [J]. Foreign electronic measurement technology, 2020, 39 (6): 1-4.

[3] Li Pengbo. The design of high rate arbitrary signal generator based on DDS [D]. BEI JING JIAOTONG UNIVERSITY, 2019.

[4] Wang Ren. Design and Realization on the Frequency Synthesizer Based on DDS [D]. Xidian University, 2017.

[5] LIU Ya-di. DEVELOPMENT OF SYNCHRONOUS TIMING GENERATOR BASED ON DDS [D]. Southeast University, 2019.

[6] Miao Zhonghua, Li Hui, Gao Jian, etc. Incremental PID Closed-loop Control Algorithm Based on DDS is Implemented in FPGA [J]. Industrial control computer, 2017, 30 (8): 35-36.

[7] XIAO YIHAN. Design and Implementation of Controlled Signal Generator using FPGA based on DDS technology [D]. Hunan University, 2008.

[8] Shen Hui, Xue Bing, Tang Chaoyang, etc. Design of signal generator based on DDS technology [J]. ELECTRONIC MEASUREMENT TECHNOLOGY, 2020, 43 (20): 160-164.

[9] HAN Shuo, JIA Dan-ping, ZHANG Tao, et al. Power Supply Design for Piezoelectric Driving Device based on DDS Signal Generation Principle [J]. Communications Technology, 2020, 53 (4): 1024-1031.

[10] Zheng Jianfeng, Bai Bichao, Zhang Han. Multi-channel drive system of phased array based on DDS chips [J]. Applied Acoustics, 2021, 182.

[11] FAN Zhiyong, ZHANG Tong, LIU Tao. Research on Configuration Monitoring Technology of Aircraft Electromechanical System Based on DDS [J]. Computer Measurement & Control, 2021, 29 (8): 104-108+113.

[12] WANG Zhicheng, PANG Yu, LIN Jinzhao, et al. A Design of Household Ultrasonic Therapeutic Apparatus Based on DDS [J]. PIEZOELECTRICS & ACOUSTOOPTICS, 2021, 43 (2): 170-173.

[13] TONG Chen-jie, PING Yi, HAN Ming-ming, et al. Research on the Fast Detection Device of the XMACII based on DDS [J]. Equipment operation and maintenance, 2021, 3: 142-143.

[14] LI Guang-yong. Design of PLC Variable Frequency Pulse Output Controller Based on DDS [J]. Automation technology and Application, 2021, 40 (7): 70-71+120.

[15] SU Li, MAO Cheng, SHEN Chunhe, et al. Research on Turbine Governor Performance Testing Device Based on DDS and Virtual Instrument Technology [J]. Hydropower and Pumped Storage, 2021, 37 (3): 54-57+62.

[16] ZHANG Qiang, CUI Yongjun. Design of frequency characteristic tester based on FPGA and DDS [J]. Electronic Design Engineering, 2021, 29 (7): 129-133.

Biography

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