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# Evaluation of a new hybrid technique based on DTMOS and PFA to improve supply voltage and power consumption of a class-AB amplifier

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**Abstract:** In this paper, two useful techniques of Dynamic Threshold Voltage MOSFET (DTMOS) and Positive Feedback Amplifier (PFA) are investigated separately and are applied simultaneously on a Class-AB Amplifier in the 180 nm CMOS technology. In the first proposed technique, Simulation results show that operating voltage can be limited to ±0.5 V in which the voltage gain and bandwidth are 52.6 dB and 103.51 MHz, respectively. In the second proposed technique, the power consumption is reduced more than 50%, the open-loop gain is enhanced 47% and Common Mode Rejection Ratio (CMRR) improves to 86.5 dB. By applying combination of these two techniques for designing the amplifier, CMRR increases to 92.1 dB and the power consumption reduces to 97 μW with the bandwidth of 59.12 MHz.

**Keywords:** Class-AB Amplifier, DTMOS, FVF, PFA.

## 1. Introduction

One of the most important parts of an electronic measurement system is its input section, (i.e., sensor). Detection of the desired input quantity and converting to an electrical signal is the most important part of such a system. Nowadays, due to decreasing supply voltage and power consumption of these circuits, achieving the minimum size and increasing lifetime of batteries, results in continuing designing electrical circuits with this approach [1].

New techniques of generation of energy from physical quantities such as light, temperature difference between two points, mechanical vibration frequency of components, moving variation, speed of rotation, etc in nanometer or micrometer scale leads to replacing batteries and power supplies with these new kinds of energy generators. Since the power provided by these generators is not high, use of low-power and low-voltage circuits is very important [2]. Hence, for detection of the desired quantities, designing operational amplifier (Op-Amp) and electronic circuits should be done with the goal of achieving high voltage gain in low operating voltage and power consumption. Applications such as portable and low power measurement systems, especially communication and wireless applications, exhibit importance of usage of low voltage and low power consumption circuits these systems [3].

In [4], Sarbishaei *et al.* use positive feedback for increasing the voltage gain. However, they couldn't achieve low operating voltage and power supply. Also, in [5] Lopez-Martin *et al.*, employ combination of local common mode feedback (LCMFB) and super class-AB OTA (operational transconductance amplifier) for increasing voltage gain and bandwidth in three circuits with different types of supply circuits in the internal stage.

Class-AB operational amplifier is one of the circuits that can be used in low voltage and low power consumption circuits [6]. In order to achieve this, in this paper two

techniques of dynamic threshold voltage MOSFET (DTMOS) and positive feedback amplifier (PFA) are used separately and their combination that is the main idea of this paper are applied on a class-AB operational amplifier. In continue, simulation results are compared with those reported in [4] and [5].

## 2. Theorem

Detecting and measuring required quantities and also minimizing the operating supply voltage leads to usage of energy provided by physical components in nanometers sizes. Fig. 1 shows the block diagram of a wireless sensor [3]. In this structure the required power for driving internal parts is provided by an electrical generator and is managed for usage of internal components of the sensor. Structure of the detection part and converting the input quantities to an electrical signal should be designed very well to operate in the following conditions:

- When achieved voltage from energy generator is not enough.
- When size of wireless sensor due to specific applications and low power should be decreased.

Hence using techniques for decreasing supply voltage is useful that are discussed in this paper later.

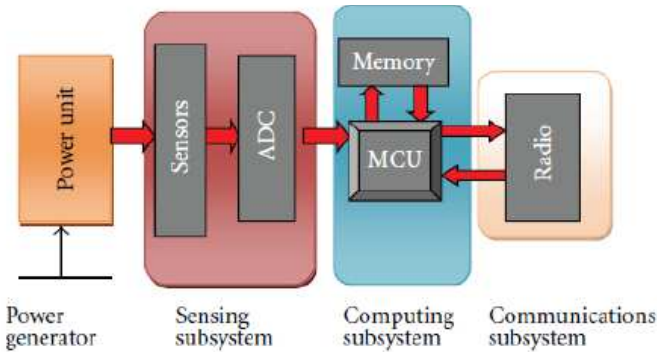


***Fig. 1.*** *Internal structure of a wireless sensor[3].*

### 2.1. DTMOS Technique

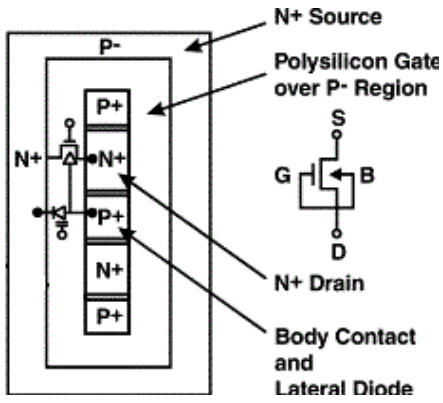


***Fig. 2.*** *DTMOS internal structure in a CMOS Transistor [8].*

DTMOS Technique has been proposed with the goal of decreasing $V_{th}$ and off-state leakage current. However, it can be used when transistor is in the saturation region. As seen in Fig. 2, in this technique the gate and body terminals are connected together and the input signal is applied to these terminals. If $V_{BS}>0$, $V_{th}$ decreases according to (1).

$$V_{th} = V_{th0} + \lambda(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|} \quad (1)$$

in which $V_{BS}$ is source-body voltage of the transistor, $V_{th0}$ is the threshold voltage when $V_{BS}=0$, $\lambda$ is the body effect coefficient, $\varphi_F$ is the Fermi potential (that has a value between 0.3 to 0.4 V) [7]. In Fig. 3, the input signal is applied to the gate and body terminals of $M_1$ and $M_2$ which are biased in DTMOS structure.

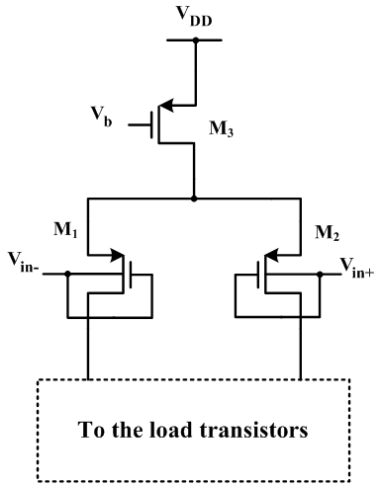


***Fig. 3.*** *DTMOS structure used in an Op-Amp input stage*

Since lower voltage (compared to the case input signals are applied to the gates of transistors) is needed for driving transistors, we expect that input voltage range increases in the common mode and also the bias current decreases, resulting in saving power [8-9].

### 2.2. Positive Feedback Amplifier (PFA)

There are different techniques for increasing the output impedance and voltage gain such as cascading transistors, Gain Boosting and Positive Feedback Amplifier (PFA). In the first and second approaches, at least extra four transistors are needed and voltage swing is limited. Hence, these techniques cannot be employed in low voltage applications [10].

In the PFA technique, due to achieving negative conductance coefficient and also high output impedance, we can expect maximum output voltage swing and high DC voltage gain [11].

Fig. 4 shows the structure of a differential PFA. Equivalent circuit for this circuit, is presented in Fig. 5. In this schematic, feedback factor is $g_{m2}$ and the closed-loop gain can calculated as following:

$$A_{CL} = (\frac{vo}{vi})_{CL} = g_{mi} A_{OL} \Big/ (1 - \beta A_{OL}) \quad (2)$$

It is obvious that if $\beta A_{OL} \approx 1$, a high gain is achieved. This condition doesn't cause instability due to the negative

feedback used in the Op-Amp [4].

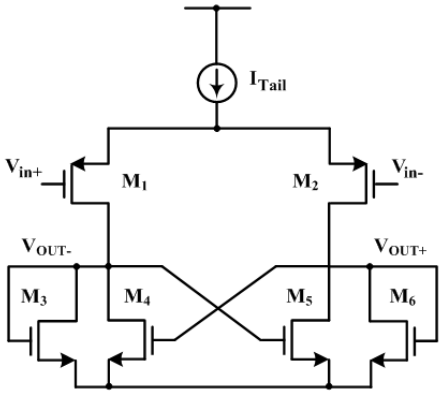


***Fig. 4.*** *Schematic of a differential PFA*

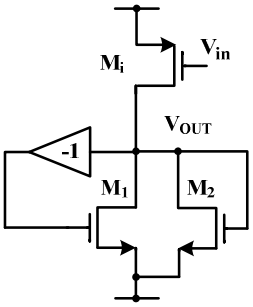


***Fig. 5.*** *Half equivalent circuit of a differential PFA*

To achieve high gain, this factor can be used as following:

$$\beta A_{OL} = g_{m1} + g_{o1} + g_{o2} + g_{oi} \quad (3)$$

It is worth mentioning that using this technique, high gain can be achieved without using cascading technique or cascading amplifier stages. Also, there is no need to the common mode feedback (CMFB) due to combination of $M_4$ and $M_5$.

### *2.3. Flipped Voltage Follower (FVF)*

A simple Flipped Voltage Follower (FVF) configuration is seen in Fig. 6. This structure can be used as a voltage shifter or buffer. In this structure, the output current depends on the current passing through the main input transistor ($M_{FVF}$). Hence, by approaching to $V_{SG(MFVF)}$, the gain becomes 1 [4].

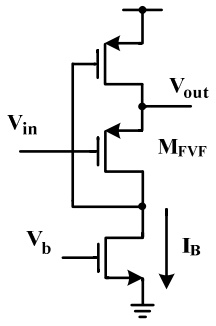


***Fig. 6.*** *Simple FVF structure*

The most important feature of this structure is its low output impedance (20 to 100 Ω) that makes it suitable for use in negative feedback structures [5]. This structure can be employed as the input stage in an Op-Amp that is shown in Fig. 7. In this circuit, current passing through $M_2$ increases when $V_{i-}>V_{i+}$. In this case, the gate voltage of $M_2$ decreases due to reducing $V_{i+}$, while its source voltage increases from another path. If this structure used in the input stage, it can increase slow rate of the amplifier.

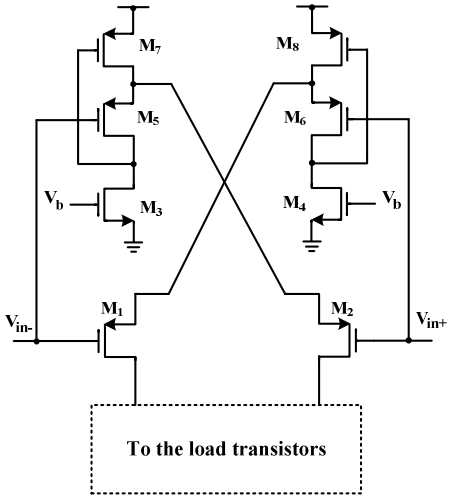


***Fig. 7.*** *FVF structure of an Op-Amp input stage*

### *2.4. Super Class-AB OTA*

Fig. 8 shows a Class-AB OTA. In this circuit, LCMFB is used for current stabilizing in main transistors. In order to increase bandwidth of the circuit and slow rate, two resistors are used in this structure [2]. Combination of $M_4$ and $M_5$ cause these transistors to operate in the ohmic region. Slow rate nan calculated by $SR = I_{Bias}/C_L$. For incraesing the solw rate, we need to increase $I_{Bias}$ which leads to more power dissipation. If this current is choosen low, the static power decreases. Size of $R_1$ and $R_2$ should be selected such that suitable phase margin is achieved. Using this technique, Autors in [4] can improve the slow rate 3 times compared to a conventional OTA.

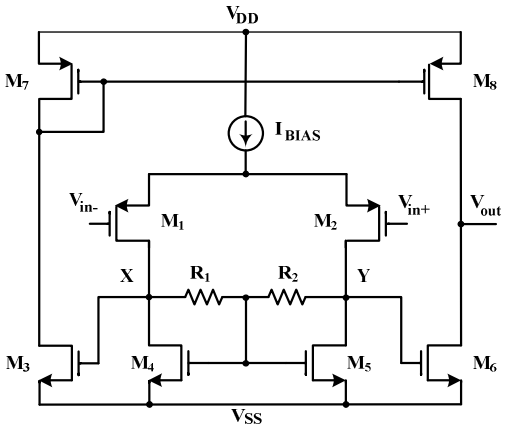


***Fig. 8.*** *Class-AB OTA circuit*

When common mode (CM) input is applied in this circuit, current passing through resistors becomes zero and voltage of $M_3$ nad $M_6$ becomes equal. In this condition, $I_{Bias}$ is devided between $M_1$ and $M_2$ equal. If differntial input is applied to the circuit, the currents of resistors and hence voltage of X and Y nodes become different.

When $V_i=V_{(i+)}-V_{(i-)}$ is applied and $I_d=I_1-I_2$ is generated, a current is produced throughout resistors. Maximum difference between X and Y nodes can be calculated by:

$$\Delta V_{GS}^{MAX} = RI_{Bias}/2 \tag{4}$$

Calculated voltage difference in the above equation produces maximum voltage swing in current of the output stage. DC open-loop gain can be writhen as:

$$A_{OpenLoop} = g_{m2}R_Y g_{m6}R_{out} \tag{5}$$

in which $R_Y$ is impedance of the Y node and $R_{out}$ is impedance of the output node. Also, $R_Y$ can be expressed by:

$$RY = R\|r_{o5}\|r_{o2} \tag{6}$$

Furthermore, resistor R can determine the maximum output current that is:

$$I_{Out}^{Max} = \beta(V_{DS4,5} + \Delta V_{GS}^{MAX})^2 \tag{7}$$

It is worth mentioning that in the differential mode, gates of $M_4$ and $M_5$ are grounded and parasitic capacitances don't affect X and Y nodes. In Fig. 8, generated differential current is proportional to $V_{id}^2$[11-12]. Also the output current is proportional to $I_d^2$ and hence, it is proportional to $V_{id}^2$. Therefore the proposed circuit is a super class-AB OTA [13].

In this paper, two useful techniques of PFA and DTMOS are investigated separately and then are applied simultaneously on the implemented super class-AB OTA in the 0.18 µm CMOS technology. In order to make comparison fair, figure of merit (FOM) is calculated as follows:

$$FOM = \frac{A_{OpenLoop}.GBW}{P_d}.\frac{1}{V_{Supply}} \tag{8}$$

in which GWB is production of gain and bandwidth and $A_{OpenLoop}$ is open-loop gain[14].

## 3. Circuit Implementation

For simulating the proposed structure, first a differential class-AB OTA, -in which FVF technique is used- is implemented in the 0.18 µm CMOS technology using Hspice software. Then DTMOS technique is applied to the first stage. In this case, operating voltage is limited to ±0.5 V. Bias currents are selected 2 µA. Then without using DTMOS technique, $M_4$ and $M_5$ transistors along with $R_1$ and $R_2$ are replaced by PFA and simulation is carried out again. In this case supply voltage is ±1 V. The proposed technique in this paper is combination of two stated techniques. Using the proposed structure supply voltage can be limited to ±0.5 V and many circuit parameters are improved. Fig. 9 shows circuit of the proposed structure.

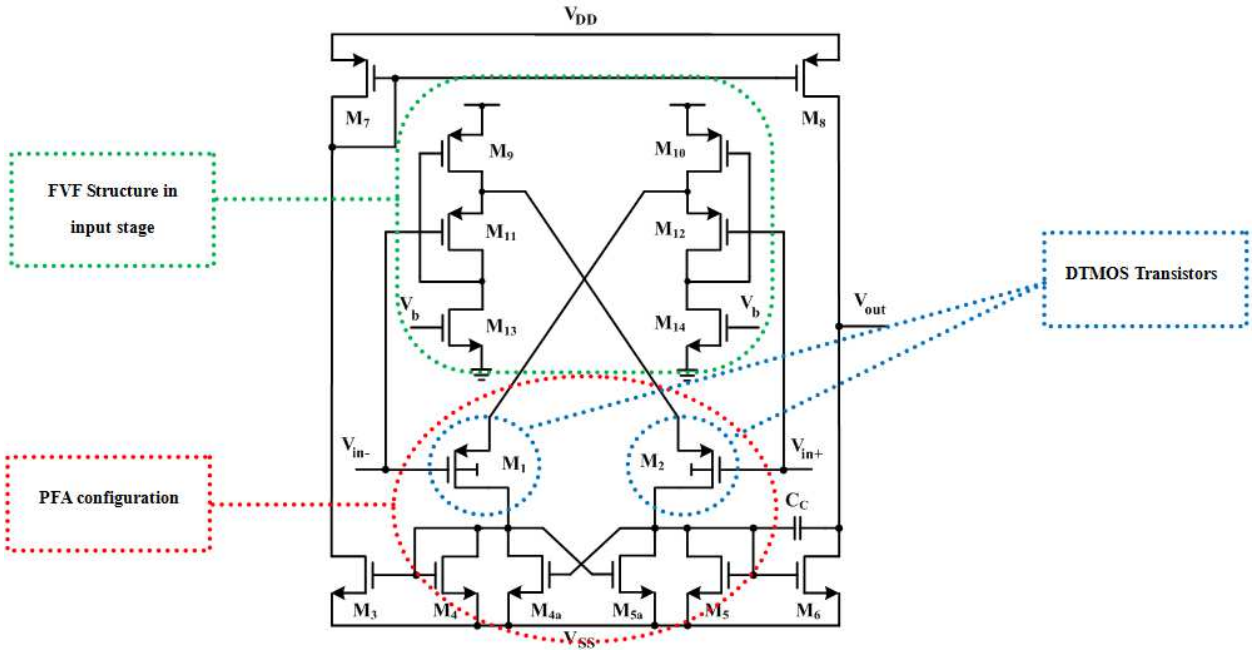


*Fig. 9. Schematic of the proposed circuit. Structure of the super class-AB OTA in which DTMOS and PFA techniques are used.*

## 4. Simulation Results

Circuits explained in the previouse section are simulated and their frequency response are demonstrated in Fig. 10. The voltage gain and bandwidth of the first circuit are 52.6 dB and 103.51 MHz.

When PFA technique is used for implementing the amplifier, the power consumption reduced more than 50%, the voltage gain improves more than 47%, and CMRR enhances to 86.5 dB. The open-loop gain and bandwidth of the proposed circuit are 77.4 dB and 59.12 MHz, respectively in which the supply voltage is ±0.5 V. Table 1 shows simulation results of DTMOS, PFA and the proposed structures and also techniques proposed in [4] and [5] (in which three bias float circuits (A), (B), and (C) are used). As observed in Table 1, the proposed circuit has the best CMRR, least power and the best FOM.

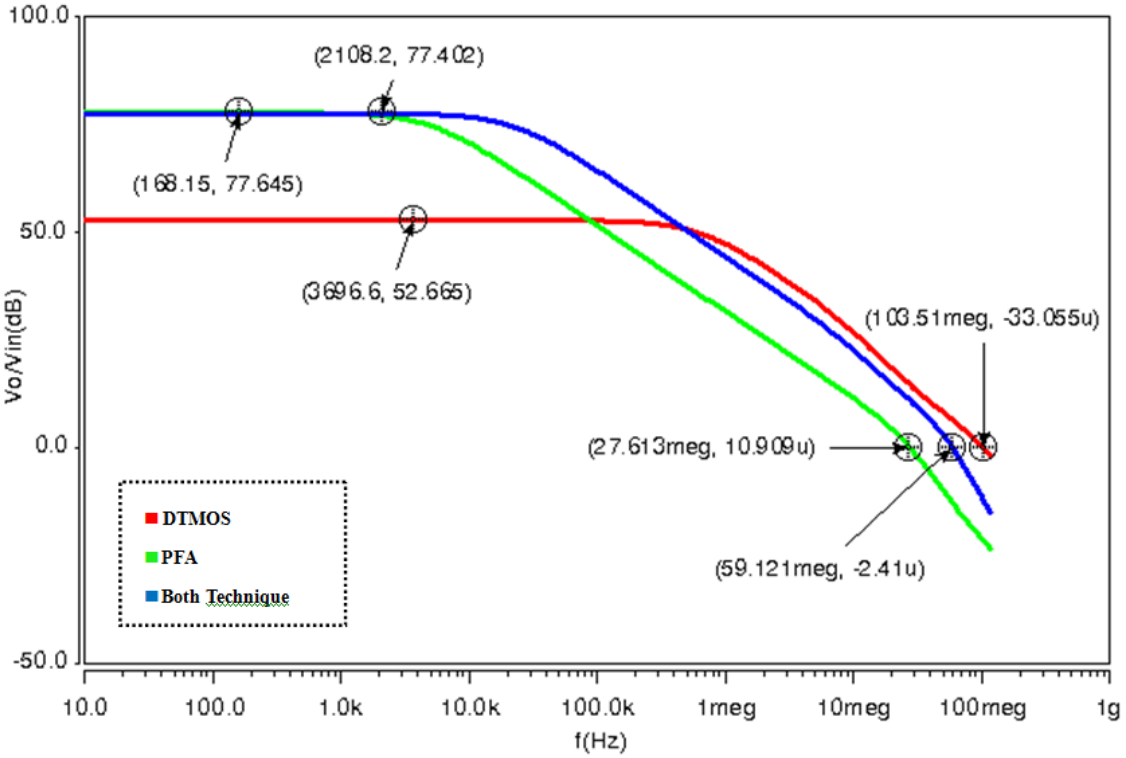


***Fig. 10.*** *Voltage gain cuves of DTMOS, PFA and the proposed technique.*

***Table 1.*** *Comparison of different techniques parameters.*

| Parameter | [4] | [5] (A) | [5] (B) | [5] (C) | Simulated [5]-(A) circuit in this paper | This Work | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | DTMOS | PFA | Proposed |
| Technology (µm) | 0.18 | 0.5 | 0.5 | 0.5 | 0.18 | 0.18 | 0.18 | 0.18 |
| $V_{Supply}$ (V) | 1.8 | ±1 | ±1 | ±1 | ±1 | ±0.5 | ±1 | ±0.5 |
| $I_{Bias}$ (µA) | -- | 10 | 10 | 10 | 10 | 2 | 2 | 2 |
| GBW (MHz) | 69 | 0.725 | 0.41 | 0.47 | 22.1 | 103.51 | 27.6 | 59.12 |
| Gain (dB) | 83.7 | 43 | 37.5 | 37.5 | 50 | 52.6 | 77.64 | 77.4 |
| Phase Margin (º) | 87 | 90 | 90 | 90 | 90 | 89 | 85 | 88 |
| CMRR (dB) | -- | 68 | 70 | 69 | 52.1 | 63.2 | 86.5 | 92.1 |
| Output Swing (V) | 1.6 | -- | -- | -- | ±0.85 | ±0.45 | ±0.85 | ±0.4 |
| Load Capacitor (pF) | 2 | 80 | 80 | 80 | 5 | 2 | 2 | 2 |
| Output Noise ($\mu V_{rms}$) | -- | 230 | 230 | 252 | 6.5 | 8 | 12 | 9.5 |
| Power (µW) | 450 | 120 | 120 | 140 | 280 | 248 | 112 | 97 |
| PSRR(+ , -) (dB) | -- | 55-58 | 50-53 | 57-46 | 86-81 | 98-80 | 80-84 | 98-86 |
| Slew Rate +/- (V/µS) | 226<br>--- | 100<br>-78 | 92<br>-76 | 42<br>-80 | 203<br>-86.5 | 148.4<br>-50 | 450<br>-177 | 105<br>-44.5 |
| FOM* | 7.12 | 0.13 | 0.064 | 0.063 | 1.975 | 21.95 | 9.56 | 47.17 |

* FOM : Figure of Merit

## 5. Discussion and Conclusion

In this paper, two practical techniques of DTMOS and PFA are investigated separately and are applied simultaneously on a Class-AB Amplifier in the 180 nm CMOS technology. In the first proposed technique, Simulation results show that operating voltage can be limited to ±0.5 V in which the voltage gain and bandwidth are 52.6 dB and 103.51 MHz, respectively. In the second proposed technique, the power consumption is reduced more than 50%, the open-loop gain is enhanced 47% and CMRR improves to 86.5 dB.

By applying combination of two techniques for designing

the amplifier, CMRR increases to 92.1 dB and the power consumption reduces to 97 µW with the bandwidth of 59.12 MHz.

Simulation result provided in the previous section proves that the proposed circuit improves many parameters of the amplifier. Decreasing operating voltage, power consumption and enhancing parameters including voltage gain, bandwidth and CMRR make the proposed structure a good choice for implementing high gain amplifiers with minimum voltage supply and also low-power portable and wireless applications.

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