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A Self-Adaptive DC/DC Buck Converter Control Modulation Design

Pengcheng Xu, Zhigang Han

Department of Electronic Science and Technology, Tongji University, Shanghai, China

Email address:
13xpc@tongji.edu.cn (Pengcheng Xu), hanzhg@tongji.edu.cn (Zhigang Han)

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Abstract: DC/DC converter is widely used in many electronic application power supplies. Usually, in the previously DC/DC converter control modulation, the duty cycle can be changed according the feedback signal in pulse width modulation (PWM) or the frequency be changed with a constant ON time or OFF time in pulse frequency modulation (PFM). A self-adaptive DC/DC converter control modulation is proposed in this paper. Based on the outputs of two uniform operational transconductance amplifiers which are influenced by the feedback voltage, both of the pulse ON time and pulse OFF time will be changed simultaneously. A self-adaptive frequency can be achieved in this control modulation. It can get a same output voltage ripple with a lower control frequency.

Keywords: DC/DC, ON Time, OFF Time, Frequency

1. Introduction

In a previously typical DC/DC converter with pulse frequency regulation (PFM) [1], usually, the OFF time of the pulse can be changed with a constant ON time or the ON time of the pulse can be changed with a constant OFF time. In the other widely used control modulation, pulse width regulation (PWM) [2], the duty cycle will be changed with a constant frequency. PWM control modulation has lower conversion efficiency in light load, while the PFM control modulation has lower conversion efficiency in high load. For a wide range high efficiency DC/DC converter, from light load to high load, dual-mode converter is been proposed previously. But there is no doubt that it increases the design complication [3-6].

A self-adaptive DC/DC converter regulation is proposed with a simple control mode. The feedback voltage from output will be used to adjust the ON time and OFF time of the pulse simultaneously. The simulation result shows that this control regulation can get a same voltage ripple with a lower control frequency under the same conditional. And also the self-adaptive frequency achieves the wide range high efficiency. Because lower switching frequency reduces switching losses.

As depicted in Fig.01, it is schematic of synchronous buck converter with self-adaptive control modulation. More and more DC/DC converter uses synchronous rectifier for its irreplaceable advantages, like fast transient response and high power density [7]. According the varying feedback voltage from output, both drive voltage pulse frequency and width will be changed. In other words, both ON time and OFF time of the driving pulse can be adjusted accordingly.

This proposed modulation is different from PWM which has a constant frequency and only can adjust pulse width, or PFM which has a constant ON time or OFF time and only can adjust OFF time or ON time respectively.

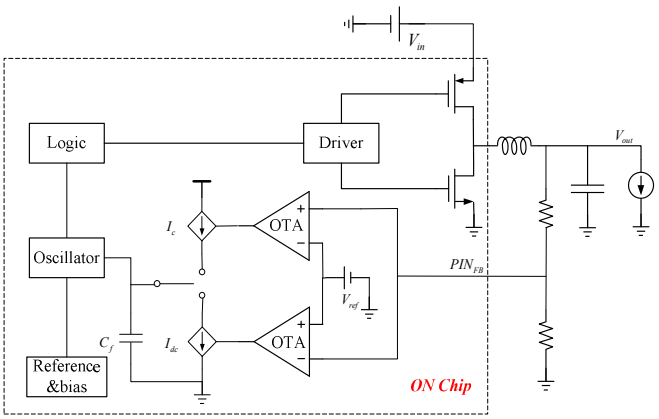

Fig. 1. *Schematic of self-adaptive control modulation buck DC-DC converter with synchronous rectifier.*

2. Self-Adaptive Modulation

2.1. Modulation Process

By the voltage sampling circuit with divided resistors, a feedback voltage $V_{feebback}$ can be generated according the varying output voltage V_{out} and transfer into the chip.

The operational transconduction amplify (OTA) can identify and amplify the difference between $V_{feebback}$ and reference voltage V_{ref}, As depicted in Fig.02 self-adaptive modulation schematic.

Two identical OTAs are used in the schematic. The noninverting input of one of OTAs is $V_{feebback}$, while the other one OTA's inverting input is $V_{feebback}$. The output of OTAs will be across on resistors R_{ON} and R_{OFF} through voltage followers and adjust the current. As a result, the two identical OTAs will generate two completely opposite output signals to control the charging and discharging current accordingly.

Two completely opposite outputs of OTAs will convert into relevant current which charge or discharge the capacitor C_F respectively.

The range of voltage of C_F is restrained between reference voltages V_{high} and V_{low}. Combining with logic circuit, with opposite changing currents can adjust both T_{on} and T_{off} of pulse.

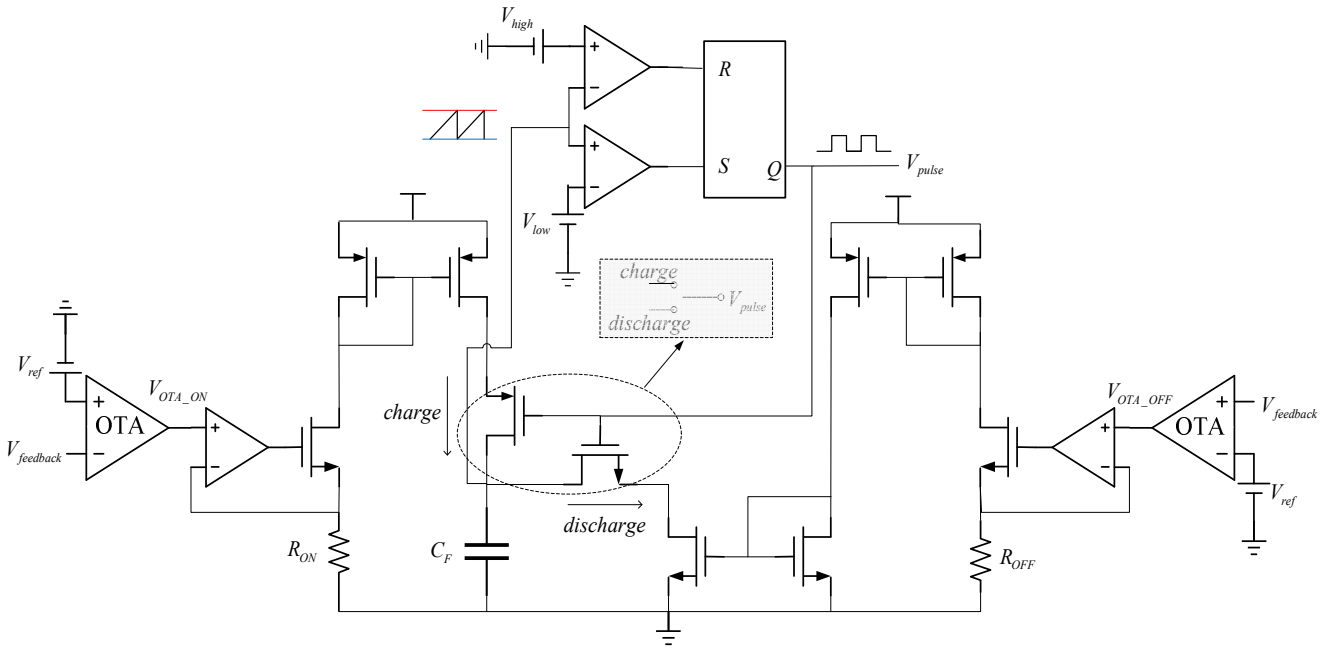

Fig. 2. *Schematic for specifying ON time and OFF of driving pulse.*

2.2. Quantitative Analysis

As depicted in Fig.02, the voltage followers can keep the voltages V_{OTA_ON} and V_{OTA_OFF} across on the resistors R_{ON} and R_{OFF} respectively. The charge current of C_F is,

$$I_{charge} = \frac{V_{OTA\_ON}}{R_{ON}} \tag{1}$$

And the discharge current of C_F is,

$$I_{discharge} = \frac{V_{OTA\_OFF}}{R_{OFF}} \tag{2}$$

As depicted in the Fig.02, the voltage across capacitor C_F rises and falls between V_{high} and V_{low}.

The switching PMOS and NMOS be turned on or turned off respectively in accordance with output voltage pulse of Set-Reset Latch. In addition, the output voltage pulse of Set-Reset Latch can control the switch of charge or discharge of capacitor C_F. Consequently, both T_{ON} and T_{OFF} will change based on varying V_{out}.

$$T_{ON} = \frac{V_{high} - V_{low}}{V_{OTA\_ON}} R_{ON} C_F \tag{3}$$

$$T_{OFF} = \frac{V_{high} - V_{low}}{V_{OTA\_OFF}} R_{OFF} C_F \tag{4}$$

$$f = \frac{1}{T_{ON} + T_{OFF}} \tag{5}$$

As depicted in Fig.03, the waveform of OFF time and ON time changing. A negative feedback for stabilizing output voltage can be achieved by adjusting the OFF time and ON time of the driving pulse at the same time.

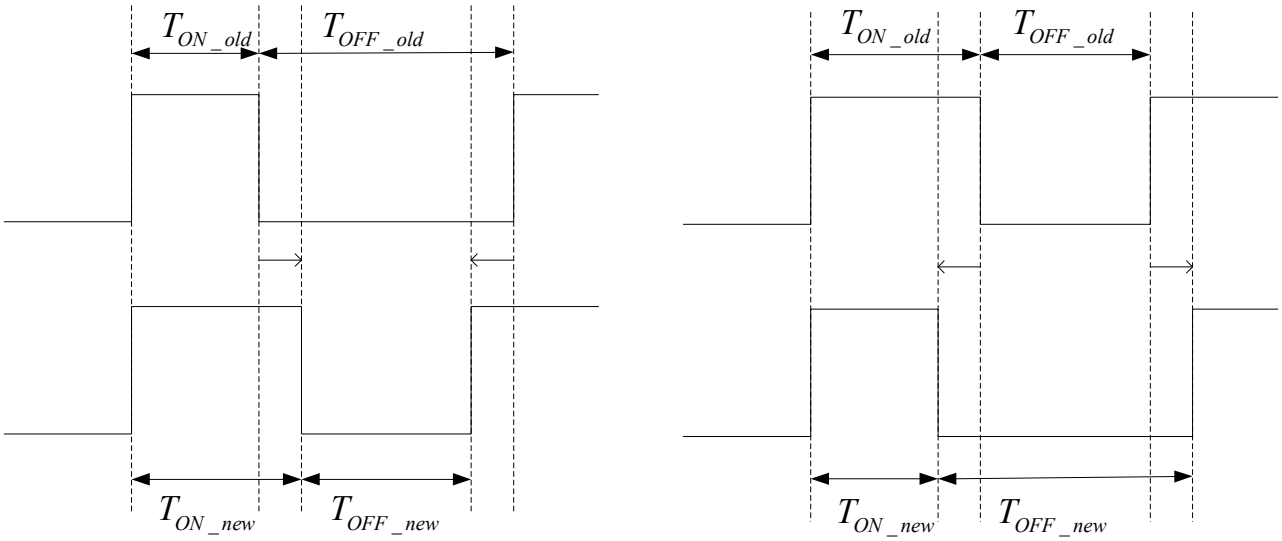

Fig. 3. *Waveform of OFF time and ON time changing according feedback voltage.*

Negative feedback control process as described following:

$$V_{out} > V_{ref} \Rightarrow V_{feebback} \uparrow \Rightarrow V_{OTA\_ON} \downarrow \text{ and } V_{OTA\_OFF} \uparrow \Rightarrow T_{ON} \uparrow \text{ and } T_{OFF} \downarrow \Rightarrow V_{out} \downarrow ;$$

$$V_{out} < V_{ref} \Rightarrow V_{feebback} \downarrow \Rightarrow V_{OTA\_ON} \uparrow \text{ and } V_{OTA\_OFF} \downarrow \Rightarrow T_{ON} \downarrow \text{ and } T_{OFF} \uparrow \Rightarrow V_{out} \uparrow .$$

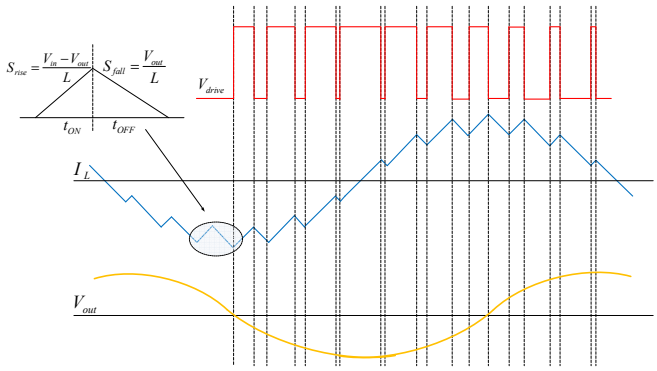

Fig. 4. *Waveform of inductor current and self-adaptive driving pulse.*

As depicted in Fig.04, the wave shape of V_{drive} has a varying ON time and OFF time. From the vertex of V_{out} to the bottom of V_{out}, the duty cycle is larger and larger until reaching to the minimum value, vice versa.

During each driving period,

When $0 < t < t_{ON}$,

$$i_{L(n)} = i_{L(n-1)} + S_{rise} \cdot t$$

When $t_{ON} \le t \le T$,

$$i_{L(n)} = i_{L(n-1)} + S_{rise} \cdot t_{ON} - S_{fall} \cdot (t - t_{ON})$$

Under the affection of filter capacitor, the output voltage can be given as,

$$V_{out(n)} = \frac{\sum_{n=0}^{n} \int_{t=0}^{t=T} i_{L(n)}(t)\,dt}{C_{fiter}} \tag{6}$$

3. Operational Transconductance Amplify

The operational transconductance amplifier (OTA) can be defined as an amplifier where all nodes are low impedance except the input and output nodes [8]. Low-impedance node always is connected to the source or gate-drain of MOS. As depicted in Fig.05, it is the schematic of operational transconductance amplifier without buffer. The resistive load is very large, almost 2Mohm. Otherwise, a resistive load will kill the gain of the OTA.

The OTA used in the schematic with a cascode low-voltage (wide-swing) current mirrors structure for increasing the magnification ability [8-10]. The terminology "1: m" indicates that N2 and N4 are sized m times wider than the N1 and N2.

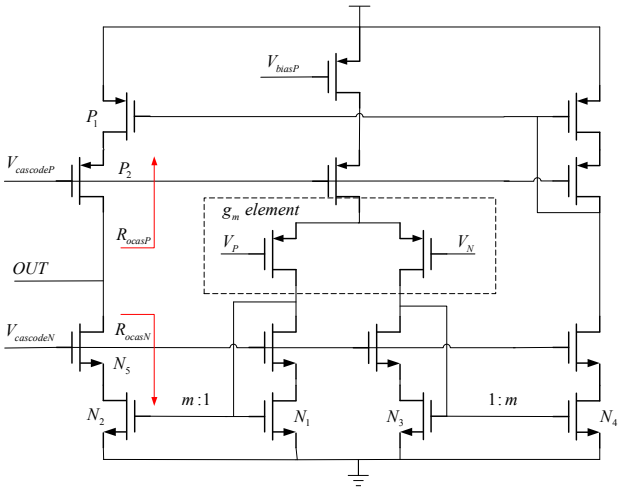

Fig. 5. *Schematic of operational transconductance amplifier.*

The low-frequency voltage gain is given by

$$A_V = \frac{v_{out}}{v_P - v_N} = m \cdot g_{mP} \cdot (R_{ocasP} \parallel R_{ocasN}) \tag{7}$$

Where the cascade resistors can be de given as

$$R_{ocasP} = (2 + g_{mP1} \cdot R_{oP1}) R_{oP2}$$

And

$$R_{ocasP} = (2 + g_{mN5} \cdot R_{oN5}) R_{oN2} .$$

The 3-dB frequency is now

$$f_{3dB} = \frac{1}{2\pi (R_{ocasN} \parallel R_{ocasP}) \cdot C_L} \tag{8}$$

For biasing the operational transconductance amplifier and other schematic, a beta-multiplier reference (BMR) is elaborately designed. The BMR is supply independent biasing for two constraint conditions without VDD specifying reference current [8].

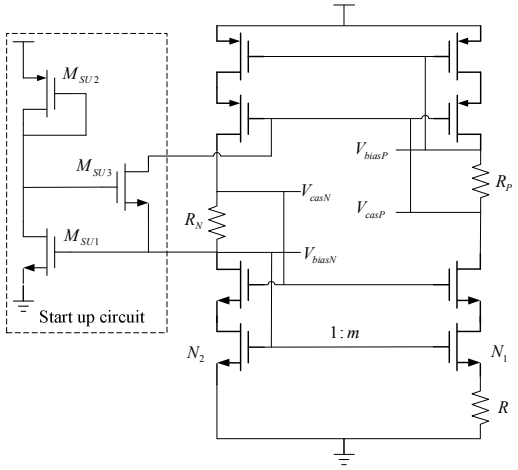

Fig. 6. *Schematic of cascode beta-multiplier reference.*

As depicted in Fig.06, PMOS cascode current mirror makes sure that both sides flow the same current. N1 is m times than N2 for smaller gate-source voltage. One of the constraint conditions is given by

$$V_{biasN} = V_{gsN2} = V_{gsN1} + I_{ref} \cdot R \tag{9}$$

Based on typical MOSFET square-law equation, there is another constraint condition given by

$$V_{gs} = \sqrt{\frac{2I_d}{\mu_n \cdot C_{ox}^{'} \cdot \frac{W}{L}}} + V_{thN} \tag{10}$$

Obviously, these two constraint condition equations don't include VDD. Combining the two constraint conditions, the biasing current of the proposed design can be expressed in the following form,

$$I_{ref} = \frac{2}{R^2 \mu_n C_{ox}^{'} \cdot \frac{W_1}{L_1}} (1 - \frac{1}{\sqrt{m}})^2 \tag{11}$$

A start-up circuit is added in the beta-multiplier reference for avoiding unwanted operating point that zero current flows in the circuit. If unfortunately, this unwanted state happens with the V_{biasN} closing to ground and V_{biasP} closing to VDD. When in this state, M_{SU1} is off and M_{SU2} turns on. A leaks current flows into N_2 from V_{biasP}. This causes the operating point converte into normal current point. After that, start-up circuit turns off and doesn't affect the beta-multiplier reference operation.

4. Current Mode Bandgap Reference

In voltage mode bandgap reference, for matching the coefficients between PTAT (Proportional to Absolute Temperature) voltage and CTAT (Complementary to Absolute Temperature) voltage, only a specified reference voltage, usually around 1.2V, can be generated. However, based on current mode bandgap reference, it has a flexible reference voltage [5, 11].

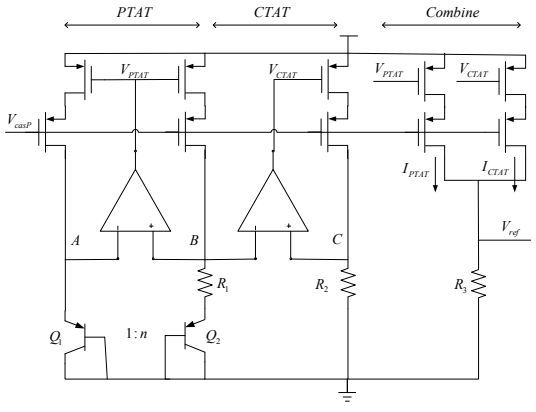

Fig. 7. *Schematic of current-mode bandgap reference.*

The two operational amplifiers, as depicted in Fig.07, forces nodes A, B and C to be at the same potential. The diode Q_2 is n time than Q_1. The PTAT current can be described as

$$I_{PTAT} = \frac{\Delta V_{BE}}{R_1} = \frac{kT \ln n}{qR_1} \tag{12}$$

Where

$$\begin{aligned} \Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= V_T \cdot \ln \frac{nI_0}{I_{s1}} - V_T \cdot \ln \frac{I_0}{I_{s2}} \\ &= V_T \cdot \ln n \\ &= \frac{kT}{q} \cdot \ln n \end{aligned} \tag{13}$$

The change in the PTAT current with temperature is

$$\frac{\partial I_{PTAT}}{\partial T} = \frac{k}{qR_1} \cdot \ln n \tag{14}$$

The CTAT current can be given as

$$I_{CTAT} = \frac{V_{BE,Q_1}}{R_2} \tag{15}$$

The change in the CTAT current with temperature is

$$\frac{\partial I_{CTAT}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g / q}{T \cdot R_2} \tag{16}$$

The reference voltage is then the sum of the PTAT and CTAT current multiplied by resistor,

$$V_{ref} = (I_{PTAT} + I_{CTAT}) \cdot R_3 \tag{17}$$

For eliminating the resistor temperature effect, the resistors R_1, R_2 and R_3 are fabricated by same poly. From the Eq.18, the temperature behavior of the resistor can be fell out from the reference voltage.

5. Simulations Result

The proposed self-adaptive buck DC/DC converter driving chip is implemented in LFoundry GmbH, Germany LF150 CMOS process. It used Cadence Virtuoso to simulate the schematic with L=500n H and C=1m F, with a 500mA 500KHZ load.

As shown in Fig.08, the simulation result meets the analysis in Fig.04. Form the simulation result, it is obvious that the DC-DC operation in current continuous mode. But driving current is considerable large. Driving PMOS and NMOS should endure so much current. It is really a challenge to MOSFETs. More deliberate design should avoid it and over current protection is needed.

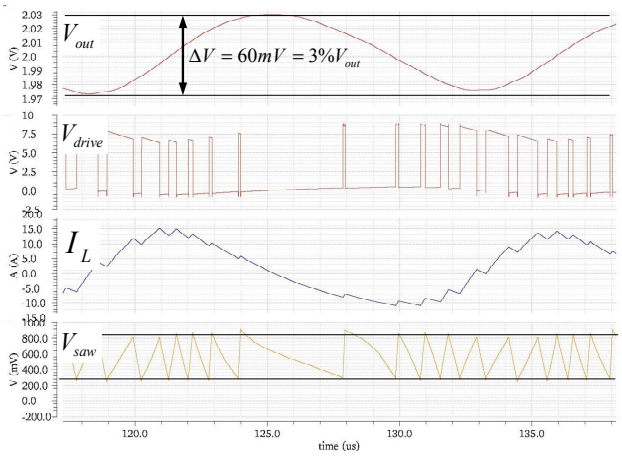

Fig. 8. *Self-adaptive DC-DC converter simulation result.*

Table 1. *Specification of the proposed self-adaptive mode control.*

Description	Value	Unit
input voltage	8	V
output voltage	2	V
load	500	mA
ripple	60	mV
Min frequency	130	KHZ
Max frequency	562	KHZ

The proposed self-adaptive buck DC/DC converter modulation can change the ON time and OFF time of the pulse simultaneously according the feedback signal. The frequency is not a constant value, but can be adaptive to the application condition. The simulation meets the design specification.

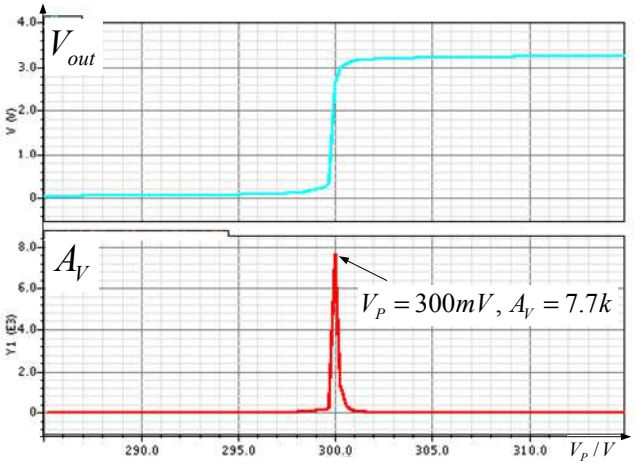

Fig. 9. *Operational transconductance amplifier simulation result.*

As shown in Fig.09, with inverting input $V_N = 300mV$, the largest voltage gain occurs at noninverting input equal to inverting input.

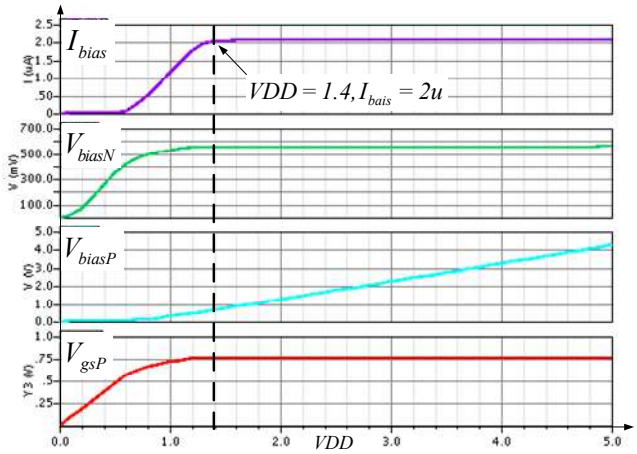

Fig. 10. *Beta-multiplier bias simulation result.*

The supply independent characteristor can be shown in Fig.10. After the circuit operating in saturation region, $VDD > 1.4V$, biasing current will be constant value 2uA. The NMOS gate-source voltage is equal to V_{biasN} being with constant. Although V_{biasP} proportional to power supply VDD, the difference between VDD and V_{biasP}, namely the PMOS gate-source voltage, also is constant.

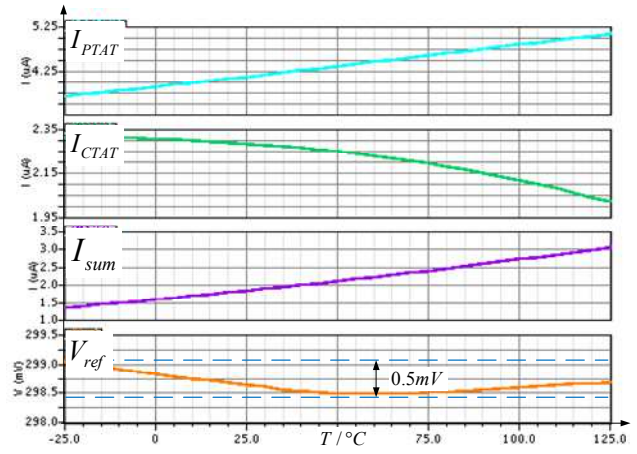

Fig. 11. *Current-mode bandgap reference simulation result.*

As depicted in Fig.11, the PTAT current has a better linearity than CTAT current. The nonlinear should be compensated in the high precise application [11]. The summing up of PTAT and CTAT current is proportional to absolute temperature. This can be counteracted by poly resistors' negative relation with temperature characteristic.

6. Conclusion

The simulations results have demonstrated the feasibility to change both pule ON time and OFF time on DC-DC converter with comparative low output ripple. It is normal that the final experimental implementation of the on-chip DC-DC converter will degrade some specifications comparative with simulation results. And also stability analysis and load transient analysis must be processed in the future before its expansion into commercial integrated circuits.

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References

[1] B. Sahu, G.A. Rincon-Mora, A accurate, low-voltage,CMOS switching power supply with adaptive on-time pulse-frequency modulation (PFM) control, IEEE Trans. Circuits and Systems, 54 (2) (2007) 312-321.

[2] Pui-Sun Lei, Chang, R.C.-H. A high-efficiency PWM DC-DC buck converter with a novel DCM control under light-load，Circuits and Systems (ISCAS), 2011 IEEE International Symposium on, pp237-240.

[3] B. Arbetter, R. Erickson, and D. Maksimovic´, "DC–DC converter design for battery-operated systems," in Proc. IEEE Power Electron. Specialist Conf., 1995, pp. 103–109.

[4] Wan-Rone Liou, , Mei-Ling Yeh, and Yueh Lung Kuo, A High Efficiency Dual-Mode Buck Converter IC For Portable Applications. IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 23, NO. 2, MARCH 2008.

[5] Biranchinath Sahu, Gabriel A. Rincón-Mora, An Accurate, Low-Voltage, CMOS Switching Power Supply With Adaptive On-Time Pulse-Frequency Modulation (PFM) Control, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 54, NO. 2, FEBRUARY 2007.

[6] Abraham I. Pressman, Keith Billings, Taylor Morey. Switching Power Supply Design. Third Edition. McGraw-Hill Professional.2009.

[7] X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module", IEEE Transactions on Power Electronics, Vol. 15, NO.5, pp. 826-834, September, 2000.

[8] R.JACOB BAKER. Circuit Design, Layout, and Simulation, Third Edition [M]. United States of America, IEEE Press, 2010:116-118

[9] Phillip E. Allen, Douglas R. Holberg, CMOS analog Circuit Design, 2nd ed. OXFORD UNIVERSITY PRESS. 2002.

[10] Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, Inc. New York, NY, USA. 2001.

[11] Charalambos M. Andreou, Savvas Koudounas, and Julius Georgiou, A Novel Wide-Temperature-Range, 3.9 ppm/ C CMOS Bandgap Reference Circuit [J]. IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 47, NO. 2, FEBRUARY 2012: 574-580.