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Reduced losses in PV converters by modulation of the DC link voltage

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Abstract: The efficiency of PV systems has improved by the fact that the researchers have used different techniques to increase their technical capabilities. This paper aims to present how the PV converter losses can be reduced by employing a polypropylene capacitor in the DC link and to modulate that DC voltage. This modification leads to problems with controllability and stability. In order to solve them two current control methods are presented - constant off time and a PWM type with second order high pass filter DC-link feedback. PV converters that utilize polypropylene capacitors do have lower losses and have lower cost. The PV converter simulation in Matlab Simulink™ and lab experiment, presented in this paper, are based on a three-phase bridge APTGF50X60T3G, used to combine a step-up/step down and H-bridge in one package.

Keywords: DC Link Voltage, Polypropylene Film Capacitors, Constant off Time Peak Current Control, PWM High Pass Filter Feedback, Cost Effective PV Converter

1. Introduction

Many manufacturers from all over the world have made the PV modules affordable, as a lot of investments, research and development has been done to achieve this. However, the total cost of a PV system also includes the cost of the inverter and the cost of installing. The grid connection cost, and installation cost still remain rather high [1], and are dependent on local labor costs. Sill, price reduction of PV systems is possible through optimization of their converters. A change in the choice of components, topology and control can be considered in order to achieve this. Many inverter technologies have been using the electrolytic capacitors in the DC link since their cost/μF has become affordable, when compared to other capacitor types. However, due to their technology, the electrolytic capacitors have a low ripple current rating [2]. For this reason, in order to reduce losses in the PV inverter technology, some companies have started to use the polypropylene film capacitors. Nevertheless, the use of these capacitors requires a good study, so that they can be used in cost-effective applications [2].

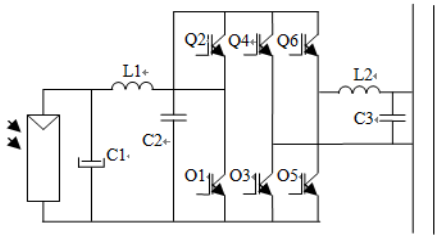

Fig 1. *Single phase PV converter using a three-phase bridge.*

Some topologies and controls have been tried out in order to reduce the losses and increase the life span of PV converters. A comparison between electrolytic and film capacitors has been carried out [3]. However, the use of a standard three-phase module for single phase injection (Fig.1) could present new opportunities in an easy assembly.

In the meantime, a configuration with a small polypropylene DC-link has been tried out. Fig.1 presents a converter topology that uses a three-phase bridge, but it uses it in a different way for single-phase injection. Polypropylene capacitors are often used in LCL filters for their large AC current capability, but here they serve as a

DC-link capacitors. The presented topology has the input inductor L_1 and the output inductor, L_2.

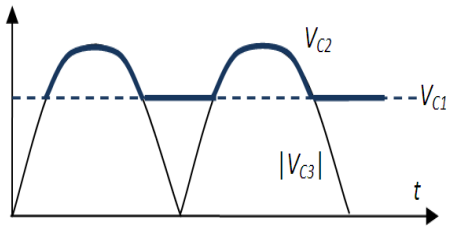

Fig 2.*Control voltage across C2 capacitor.*

The advantage of using inductors at input and output is that low current ripples are obtained. PWM is needed only for low instantaneous voltages on C3. The capacitor C1 is used here at a typical 150-250 V and is much larger in value and size than C2.

Fig. 2 shows that the voltage on capacitor C2 is almost constant when the instantaneous grid voltage is low. Q3, Q4, Q5, and Q6 make a single phase H-bridge, where C3 and L2, form a low pass filter for EMC (Electromagnetic Compatibility). In the H-bridge, Q3 and Q4 are switched depending on the quadrant whereas Q5 and Q6 are switched depending on the quadrant and PWM modulated. This allows using only one low pass inductor in the output. Fig. 2 shows the waveform on C2. Also, it is known that in a transistor module, the outer legs are better cooled than the mid-leg and can sustain slightly higher losses due to switching.

The proposed topology offers several advantages. The switching losses in Q1 are limited as the voltage across the C2 is lower than usual, and it switches only during some periods of the time. The capacitor C2 is a low loss type and the capacitor C1 is large, thus helping to reduce EMC (Electromagnetic Compatibility). The switching losses in Q5 and Q6 are limited since they do not switch during the peak of the sine.

The slow leg Q3-Q4 permits the use of only one active filter inductor L2 to lower the EMI (radio interference) from the PV to grid. However, the topology does also show some disadvantages. The control of the converter is not obvious,

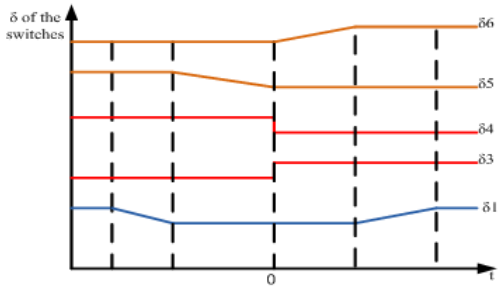

Fig 3. *The PV converter switching behavior.(x-axis: desired voltage at the output of the H-bridge. y- axis: the duty ratio of the switches to be operated.)*

because when the grid impedance is taken into account, a resonant 4th order circuit or even higher, is obtained. The reason is that C2 is a foil capacitor with low capacitance value.

The inductors L1 and L2 play a big role in the PV converter. The direct hard switching with high di/dt at the output level of the PV converter is reduced because of the presence of the inductors and the switching, which occurs at a typically lower voltage. This makes the conversion smoother and with less EMC problems. Also, the losses in C2 are very low compared to electrolytic capacitors. However, two questions remain: is the converter stable enough and can it be controlled well? This will be investigated in this paper.

Fig.3 shows the current mode control of the PV converter. The voltage at the output of the bridge is used to control the current in L2. The current control for the topology makes the system work in four quadrants. The way of control results in a multilevel action without being a multilevel converter topology.

2. Losses in a PV Converter Link

2.1. Module Conduction Losses

The losses in a PV converter can originate from different sources. One non-negligible source is the switching of the power electronic devices [3]. Since the switching occurs at high current rates, the DC link bus must have a low ESR (Equivalent Series Resistance) capacitor in order to reduce the losses. If a polypropylene film capacitor is used, the ripple current is less limiting. Instead, the voltage ripple is becoming important, but this is not a severe problem in the DC-link. The switching loss calculation of the PV converter (Fig.1) is based on the APTGF50X60T3G module data sheet and on the DC-link voltage modulation (Fig.2). However, the following equations are used to evaluate the conduction losses in the PV converter [3].

$$P_{CV,Q} = \frac{V_{CE,O}\hat{I}_L}{2.\pi}\int_0^{\pi}\sin(\omega t).\frac{1+M(t)}{2} + \frac{r_{CE,O}\hat{I}^2{}_L}{2.\pi}\int_0^{\pi}\sin^2(\omega t).\frac{1+M(t)}{2} \quad (1)$$

$$P_{CV,D} = \frac{V_{F,D}\hat{I}_L}{2.\pi}\int_0^{\pi}\sin(\omega t).\frac{1-M(t)}{2} + \frac{r_{F,D}\widehat{I_L^2}}{2.\pi}\int_0^{\pi}\sin^2(\omega t).\frac{1-M(t)}{2} \quad (2)$$

$$P_{CV} = 6\,(P_{CV,Q} + P_{CV,D}) \quad (3)$$

Where ω is the current's angular frequency, $V_{CE,O}$ is the IGBT's threshold voltage, r_{CE} is the IGBT's differential resistance, $V_{F,O}$ is the diode's threshold voltage, V_f is the diode's differential resistance and $M(t)$ is the modulation function, $P_{CV,Q}$ and $P_{CV,D}$ are conduction losses in IGBT and in diode respectively.

In the considered module, the transistor voltage drop is very close to the diode voltage drop. For the H-bridge, equations (2) and (3) show that using a lower DC-link voltage increases M(t). In the boost converter, the diode losses increase and the transistor losses decrease by almost

the same amount. So, for the total module, the DC link modulation has almost no effect on the losses.

2.2. Switching Loss Calculation

In most of topologies, the switching losses are not negligible compared to the conduction losses. The switching loss can be estimated in equation (4).

$$P_{sw} = f_{sw}\left(\int_{t_1}^{t_1+t_{swon}} i_s . V_s dt + \int_{t_2}^{t_2+t_{swoff}} i_s . V_s dt\right) \quad (4)$$

Where, f_{sw} is the switching frequency, i_s and v_s are respectively instantaneous current and voltage through the IGBT, t_1 is the IGBT ON starting time, t_2 is IGBT OFF starting time, t_{swon} is the IGBT ON time and t_{swoff} is the IGBT OFF time. One can see that the losses are rather proportional to the frequency and voltage. E_{on} (Turn On Energy loss) and E_{off} (Switching off Energy) are given by the manufacturer [4]. Some overall optimizing result was achieved by considering the switching frequency of 25 kHz. However the optimal choice is quite flat. The frequency is a tradeoff between switching losses, EMI and inductor losses.

2.3. Losses in the DC Link Capacitors

The DC link losses in C2 are mainly depending on the high frequency current in C2, which is in the order of 10A rms for the considered power. Typical electrolytic capacitors may have an ESR at 10 kHz of about 50 mΩ in hot condition, and significantly more in cold. A polypropylene capacitor such as MKP1848S has an ESR of 17 mΩ, and 8.5 mΩ when two are used in parallel. Also their price is about 10 times lower. In the proposed converter, the losses in C1 are mainly 100Hz losses. These losses are still present due to the fact that the power to the grid pulsates with 100Hz in the grid. However, the high frequency current ripple in C1 is low. Moreover, it is possible to oversize C1 without start-up problems as the capacitor is charged by the PV and not by the freewheel diodes of the H-bridge and the grid. The ripple on C1 is used afterwards for MPPT (Maximum Power Point Tracker).

3. Constant off Time Peak Current Control

3.1. Principle

Current mode control at constant frequency is well known method, but it has a risk of instability at half of the switching frequency. If the frequency is not kept constant, several outcomes are known [5]. Here, the "constant off time peak current control" (COPCC) is chosen since it has the advantage to include protection in the same item as the control. It switches off when the set current is reached and then a fixed off time is applied. In contrast, the COPCC is stable for all duty ratios (Fig.4), but it does not keep the frequency constant. This type of control is often used in LED (Light Emitting Diode) converters and is also good in motor control [6]. Fig. 4 shows the principle of the COPCC. Note that the duty ratio is beyond 50% without any stability problem. Other stability problems arise close to the resonance frequency, which are similar to the ones encountered in LCL output filters [7],[8],and [9].

3.2. Simulation

Fig.5 presents the principle circuit of the COPCC. The NO switch closes while the input goes high. The elements in circuit were calculated in order to get 25 µs off time. The resulting output resembles a retriggerable monostable multivibrator.

Fig.6 presents the principle circuit of the constant off time peak current control circuit with high pass filter feedback on the voltage of C2, to damp resonances on C2. The idea is that the high pass filter compensates for the phase delay at the resonance frequency. This way, one can actively damp the resonance. In the case of the COPCC, the averaged phase delay is in the frame of half a period of the frequency for this type of control.

The simulation was performed based on the values of Table I. The simulation goal is to test the dynamic of the DC link of the PV converter topology using the naked COPCC (Fig.5) and the COPCC with high pass filter feedback (Fig.6). Adding a high pass filter feedback (Fig.6) into the constant off time current control, improves the stability of the system (Fig.8) and (Fig.9). The input voltage is 100 V and the output voltage is 200 V. The current reference as voltage image is 6 Amps with superimposed square wave of 1 Amp amplitude, and a frequency of 125 Hz.

Table 1. *Converter components.*

Material	Type	Value
Capacitor, C1	electrolytic	2200 µF
Capacitor, C2	Polypropylene film	20 µF
Capacitor, C3	Polypropylene film electrolytic	2200 µF
Inductor, L1	Amorphous iron	500 µH
Inductor, L2	Amorphous iron	1400 µH
IGBT	APTGF50X60T3G	-
DC source V1		100V
Load	Resistive	50 Ω

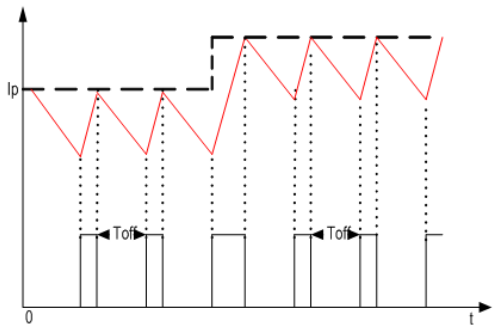

Fig 4. *Constant off Time Peak Current Control.*

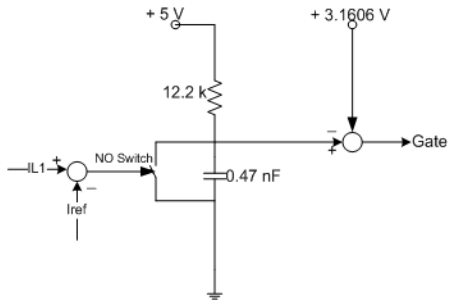

Fig 5. *Constant off Time Peak Current Control Circuit.*

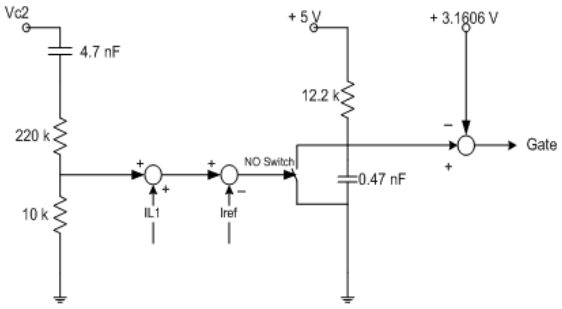

Fig 6. *Constant off Time Peak Current Control Circuit with high pass filter feedback.*

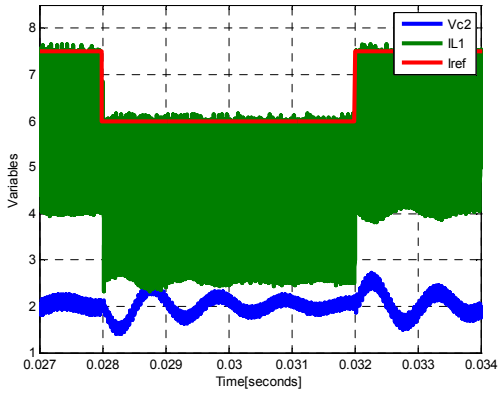

Fig 7. *Current in L1 and DC-link voltage using Constant off time Peak Current Control without feedback.*

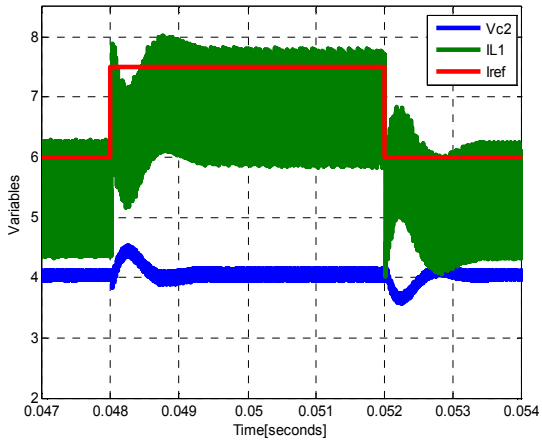

Fig 8. *Current in L1 and DC-link voltage using Constant Off time peak current control with HPF feedback.*

Fig.7 shows the response. Moreover, it shows that there is some resonant frequency. However, constant off time peak current control with HPF feedback stabilizes the system (Fig.8). In this way the system is being damped and has a reasonably fast step response. To simulate the low impedance of the grid, an electrolytic capacitor was put at the output.

3.3. Lab Experiment

The step-up is mainly composed of the power stage (top side), the constant off time current control (middle part), and the over voltage protection (bottom part) (Fig.9). In the step up mode, the system is stable without feedback, whereas in the step down mode, the system is even unstable in open loop. In Fig.10 and 11, the measured signals are shown, where channel 2 is the current, the purple channel is reference current and yellow channel is the voltage. The lab results and the simulation show a similar dynamic behavour of the system. Fig.10 and Fig.11 show that the output voltage is 178V, with an input voltage of 89V. The response in Fig.7 has the same dynamic behavior as the response in Fig.10. Similarly, the response in Fig.8 and Fig.11 are quite the same.

The constant off time peak current is fast but it is not easy to implement it using a microcontroller in order to operate in four quadrants (Fig.3). It also has another drawback: that the current in L2 cannot be controlled directly when switching the left leg. For these reasons, the paper presents another technique, PWM high pass filter feedback, which can be more powerful than the previously discussed method. It is not discussed here, but it is shown that the control of a step down converter in current mode control is unstable due to L1 and the small C2. In experiments, the circuit goes in overvoltage protection.

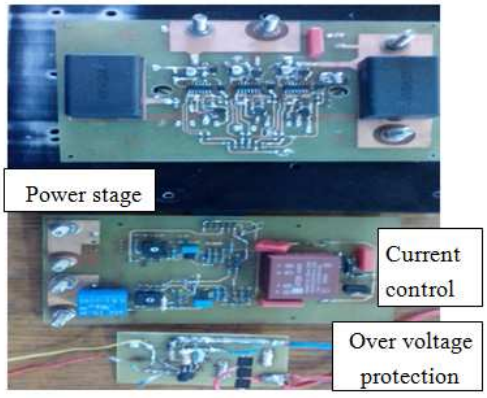

Fig 9. *Buck-Boost Converter Step Up.*

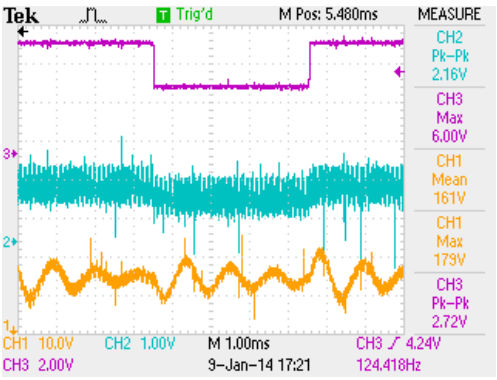

Fig 10. Constant off time Peak Current Control without HP feedback.

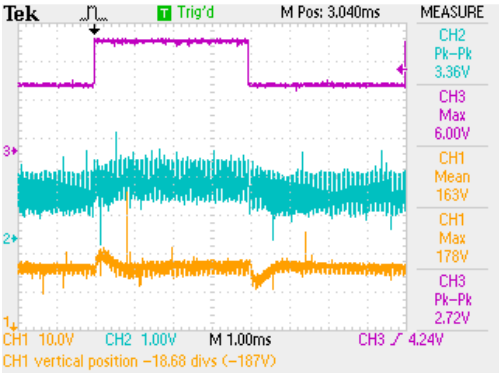

Fig 11. Constant off time peak current control with HP feedback.

4. PWM High Pass Filter Feedback

4.1. PWM Simulation Build up

Digital circuits are quite convenient for power electronics [10]. Some digital circuit limitations, PWM resolution and so on, are not anymore a challenge because with a good design and selection of microcontrollers it is possible to overcome them. The current control described in this paper is based on the control of the duty ratio of the boost and buck-boost converter (Fig.12). While damping the resonance in C2, it is possible to do more: digitally, it is easy to control I_{L2} directly while one is controlling δ1 where the peak current control is controlling only I_{L1}, and it would still need further control operations such as feed forward. The main drawback of digital control is that a delay due to sampling is introduced during its conversion to digital, calculating and applying it to compare with a saw tooth.

Typically there is about one period delay in the control of a duty ratio, and even more in current control. An equivalent low pass LCL circuit has typically almost no phase shift at low frequency and 180° phase lag at high frequency. So, to damp the resonance, a 90° phase lead should be given. Also some phase advance to compensate for the delay of the processor based PWM should be considered. To obtain that one needs a second order high pass filter. On one hand it is not so obvious to implement it digitally as the calculation of second order high pass filters needs several samples and time. On the other hand it is difficult to absorb it in a PID controller.

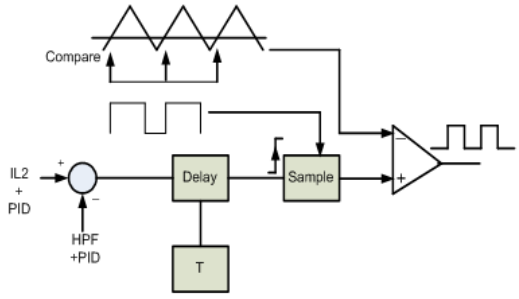

***Fig 12.** Sampled PWM Block Diagram IL2.*

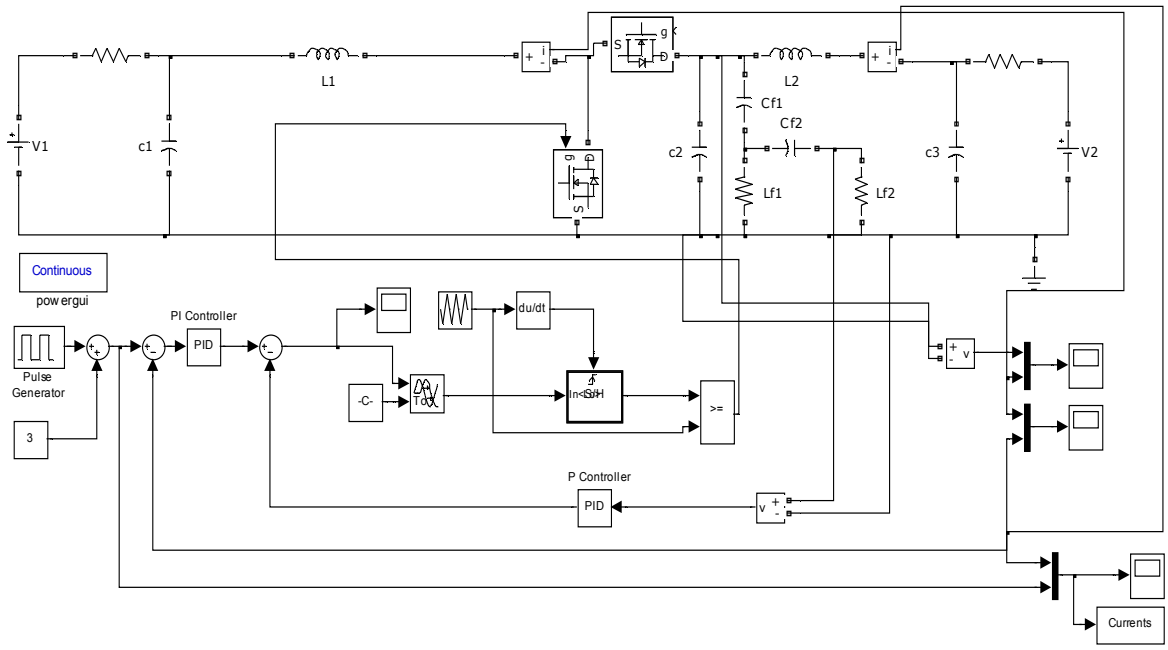

***Fig 13.** The PV converter current mode control block diagram simulation: Boost converter mode.*

Normally, it is expected that the DC-link voltage must be measured. However, the second order HPF of the DC-link voltage is directly sampled instead of sampling the DC-link voltage. This saves time and is more accurate. The second order limits the amount of disturbance on the measured signal, compared to a pure digital differentiating action.

4.2. PWM High-Pass Filter Feedback Simulation

Table I shows the values that were used to test the DC link of the PV converter. Both step-up and step-down are tested. Fig.13 presents the circuit diagram of the converter. The C2 value was changed from 20 µF to 10 µF in order to tune easily the control. The high pass filter damps all resonant frequencies from the DC-link. The grid is modeled as back EMF.

As the PV converter hosts three parts: Step-up DC converter and step-down DC converter, and H-bridge, it is convenient to test each part separately.

Therefore, the step-up converter is simulated first and after that the step-down is simulated as well. Fig.13 shows the boost converter current-mode control using the second order high pass filter. The time constants are 30 µs and 60 µs for the first and second high pass filter, respectively. On one hand, the current control has only proportional and integrating functions. On the other hand, the second order high pass filter PID is in fact only a proportional active controller. The results of the controller are found in Fig.14 and Fig.15. From Fig.14, it is obvious that the step response of the system is stable. It is even fast if the parasitic resonance of C2 is taken into consideration. The reference current is a step function (Fig.14). In another part of the period, to control the same current I_{L2} using δ2 was as well successfully simulated with the same PI controller (Fig.15). All in all, the simulation tests of both converters (step-up and step-down) reveal that the control of the H-bridge can be easily achieved. In other words, it is obvious that the whole system can work as long as the DC-link voltage is well controlled. It must be emphasized that the current in L2 can be controlled by using the same high pass filter feedback for the damping, for both boost and H-bridge operation, although different transistors are controlled. However, between both modes of Fig. 14 and 15, the gain of the PI and P controller have to be slightly adapted.

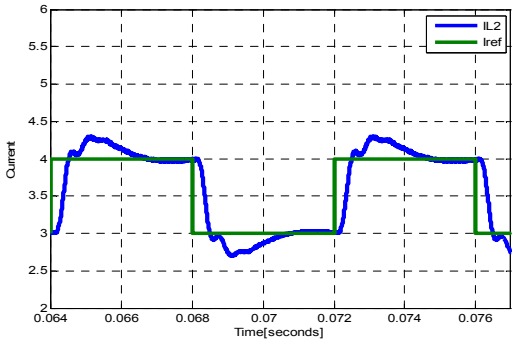

Fig 14. *I_{ref} and I_{L2} while controlling the boost converter.*

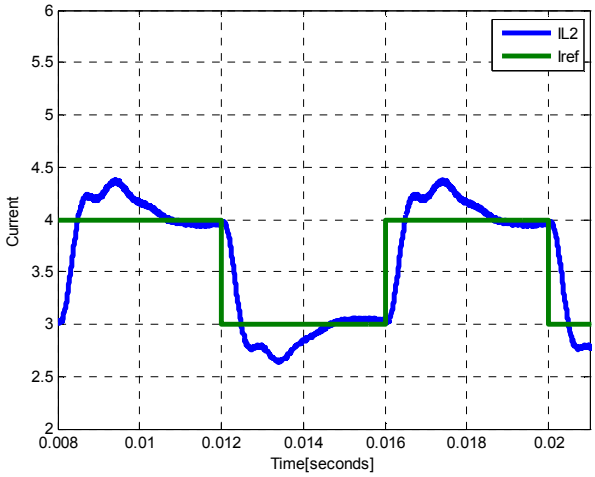

Fig 15. *I_{ref} and I_{L2} while controlling the step down converter.*

5. Future Work

Up to now, it has been shown that the control of both buck and boost parts can be stabilized and that the current in the inductor L2 can be controlled. The future work will be to implement, the control of the four quadrants of the inverter by employing the PWM high pass filter feedback control according to (Fig.3).

6. Conclusions

For single phase grid injection, a three-phase bridge topology can be used while using the left leg as a boost converter and implementing a reduced, film type DC-link capacitor. However, the behavior tends to have a pronounced resonance for the step-up converter; for the H-bridge it is even unstable. On one hand, this pronounced resonance can be damped with the application of an analog constant off time peak current control using a first order high frequency filter to stabilize the resonant frequency. On the other hand it can be controlled by a fast duty control in a digital processor, while making a feedback during the sampling of a second order high pass filter. At low instantaneous grid voltage, the H-bridge is modulated. When the grid voltage is higher than the DC input voltage, the current to the grid can still be controlled with the step-up converter without switching in the H-bridge. The controllability of the current reduces the switching losses of the PV inverter.

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References

[1] Lucas Laursen, "Production of Solar Panels Outpaced Investment Last year", 1 Oct 2013 http://spectrum.ieee.org/energywise/energy/renewables/production-of-solar-panels-outpaced-investments-last-year.

[2] S. Michael and B. Joe "Selecting Film Bus Link Capacitors for High Performance Inverter Applications," Electronic Concepts Inc.Eatontown, NJ 07724.

[3] M.H. Bierhoff, F.W. Fuchs, "Semiconductor Losses in Voltage Source and Current Source IGBT Converters Based on Analytical Derivation," Vol.4 PESC04,pp.2836-2842.

[4] http://www.digikey.com/product-detail/en/APTGF50X60T3G/APTGF50X60T3G-ND/1920455.

[5] XiangdongZong, "A Single Phase Grid Connected DC/AC Inverter with Reactive Power Control for Residential PV Application". University of Toronto, 2011

[6] Alex Van den Bossche, DimitarVaskovB.,Thomas V, and VencislavCekov V., "Programmable Logic Based Brushless DC Motor Control" EPE Aug. 30 2011-Sept. 1 Birmingham 2011, pp1-10

[7] RajendaAparnathi and Ved Yvas Dwived, "LCL Filter for three Phase Stable Inverter Using Active Damping Method (Genetic Algorithm)" e70081934. Doi:10.7392/Engineering.70081934, February, 28,2013.

[8] Antonio Coccia, "Control Method for Single-Phase Grid Connected LCL Inverter",ABB research LTD, 8553434, October,8, 2013.

[9] Daniel Wojciechowski, "Unified LCL Circuit for Modular Active Power filter", International Journal for Computation and Mathematics in Electrical and Electronics Engineering,Vol.31 Iss:6,pp.1985-1997.

[10] Jian Li, "Current-Mode Control: Modeling and its Digital Application", Blacksburg, Virginia, 2009.