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Design of an All Optical 3-Bit Modulo Eight Asynchronous Up Counter

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Abstract: The paper presents an all-optical 3 bit up counter with complete Boolean functionality as a representative circuit for modeling and optimization of monolithically integrated components. Here, the proposed logic unit design is based on nonlinear effects in semiconductor optical amplifiers (SOA).These equations are first solved to generate the pump, probe and conjugate pulses in a SOA. The pulse behavior are analyzed and applied to realize behavior of all-optical NAND gate. Next, the logic is used to implement All-Optical D Flip-Flop logic, and its function is verified with the help of truth table. Finally with the help of three D Flip-Flops, a 3-bit up counter is proposed.

Keywords: Semiconductor Optical Amplifier, Four Wave Mixing, Optical Logic Gates, Cross Gain Modulation

1. Introduction

SOAs exhibit non-linear properties due to carrier density changes induced by differences in power of the input signals. The growth of large scale integration of SOA technology offers economical, high performance devices. While these non-linear properties create problems for the use of SOAs as simple linear gain elements, they can be exploited to perform functions that are typically carried out by electronic signal processing circuits. In the case of all applications mentioned above, the data signal is processed in optical form, rather than first being converted to an electrical signal. In one sense SOA-based devices are compact, stable, integration-capable and potentially independent of polarization and wavelength [1]. Further, it has the advantages of low switching energy and low latency [2]. A computation that might take more than eleven years by the conventional electronic only one single hour [3].The use of the optical fibers as nonlinear elements in switching devices gives so high speed operation since the nonlinear response of the fiber is extremely fast and the Possibility of creating a rectangular switching by using a dispersive walk-off between the data and the control pulse but the nonlinear coefficient is usually very small in conventional fibers [4].In this paper the full logic is developed in MATLAB platform.

2. Simulation Method

If we consider $A_0(0, t)$ as input pump pulse amplitude at any end of SOA, $A_0(L, t)$ as input pump pulse amplitude at length L of SOA then from [5] we can have the following equation.

$$A_0(L,t)=A_0(0,t)e^{\left(\frac{1}{2}\right)(1-i\alpha)h}$$

Where, L=length of SOA, t=time and rest of the parameters are defined in Table1.

Again, if we consider A1 (0, t) as input probe pulse amplitude at any end of SOA, A1 (L, t) as input probe pulse amplitude at length L of SOA, $A_2(0, t)$ as input conjugate pulse amplitude at any end of SOA and $A_2(L, t)$ as input conjugate pulse amplitude at length L of SOA then,

$$A_1(L,t)=A_0(0,t)\left[e^{\left(\frac{1}{2}\right)(1-i\alpha)h-\eta_{10}|A_0(0,t)|^2(e^h-1)}\right]$$

$$\cos h\left[\left(\frac{1}{2}\right)\sqrt{\eta_{02}\eta_{01}^*}|A_0(0,t)|^2(e^h-1)\right]$$

$$A_2(L,t)=\frac{A_1^*(L,t)A_0(L,t)}{A_0^*(L,t)}\sqrt{\frac{\eta_{01}}{\eta_{02}^*}}$$

$$\sin h\left[\left(\frac{1}{2}\right)\sqrt{\eta_{01}\eta_{02}^*}|A_0(L,t)|^2e^{-h}(e^h-1)\right]$$

Where, L=length of SOA, t=time and rest of the parameters are defined in Table 1.

From [5] we also have,

$$\eta_{01}=\eta_{01}^{CD}+\eta_{01}^{CH}+\eta_{01}^{SHB}$$

Where,

$$\eta_{01}^{CD}=\varepsilon_{cd}\frac{1-i\alpha}{((1+i\Omega\tau_1)+(1+i\Omega\tau_s))}$$

$$\eta_{01}^{CH}=\varepsilon_{t}\frac{1-i\alpha_T}{((1+i\Omega\tau_h)+(1+i\Omega\tau_1))}$$

$$\eta_{01}^{SHB}=\varepsilon_{shb}\frac{1-i\alpha_{shb}}{1+i\Omega\tau_1}$$

The amplification function, h and coupling coefficient η_{ij} is defined in [6]. All other typical parameters related with InGaAsP Semiconductors and used for quantitative evaluation are listed in Table 1.

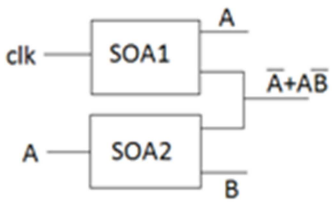
Table 1. *Parameters used in Simulation work.*

Parameters	Symbol	Values	Units
Length of amplifier	L	450	Mm
Width of the active region	W	1.5	Mm
Depth of active region	D	0.3	Mm
Traditional confinement factor	Γ	0.3	
Small signal gain	g_0	1.54×10^{-4}	m^{-1}
Saturation power	P_{sat}	28.4	mW
Carrier lifetime	$_s$	300	Ps
Nonlinear gain compression for carrier heating	$_t$	0.13	W^{-1}
Nonlinear gain compression for spectral hole burning	$_{shb}$	0.07	W^{-1}
Traditional Line width enhancement factor	A	5.0	
Temperature Line width enhancement factor	α_T	3.0	
Line width enhancement factor for spectral hole burning	α_{shb}	0.1	
Time for carrier carriers cattering	$_1$	50	Fs
Time for carrier photon scattering	$_h$	700	Fs
Carrier depletion coefficient	$_{cd}$	47	W^{-1}

3. Result and Discussion

By using the equations mentioned above in MATLAB environment we can obtain the pulses for probe, pump and conjugate signal.

In SOA1 Pump 'A' saturates the gain of probe 'clock', resulting in conjugate of Pump 'A'. Also in SOA2, Pump 'B' saturates the gain of Probe 'A', which inverts the signal 'B' and on multiplication with 'A' result in, product of 'A 'and inverted 'B' signal. The resulting signal is the sum of outputs of SOA1 and SOA2 will result a NAND output, which can be verified with the help of waveforms and truth table.



(a)

A	B	$Y=A\bar{B}+\bar{A}$
0	0	1
0	1	1
1	0	1
1	1	0

(b)

Fig 1. *(a) NAND Gate using SOA's (b) Truth table of NAND Gate.*

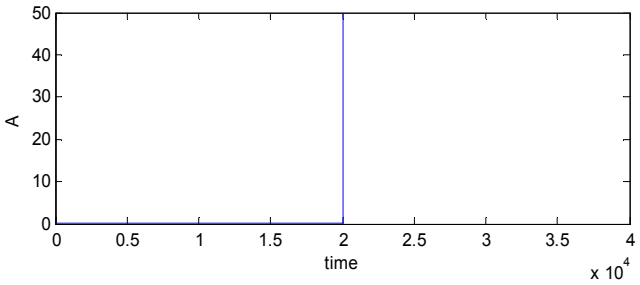


Fig 2. *Input A taken as [0 0 1 1].*

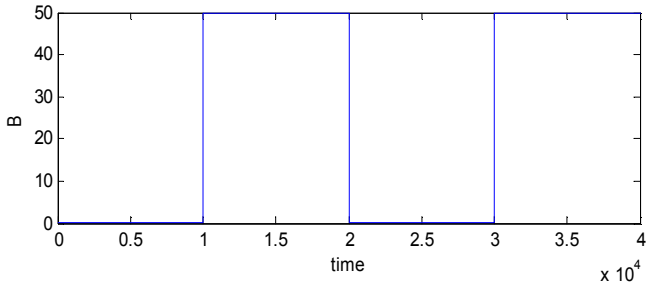


Fig 3. *Input B taken as [0 1 0 1].*

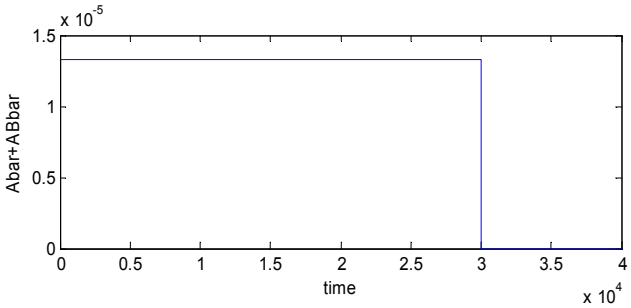


Fig 4. *Output of NAND gate obtained as [1 1 1 0].*

The above waveforms show that when values of input A and B are taken as [0 0 1 1] and [0 1 0 1] respectively and on applying clock as [1 1 1 1] the final output of waveform is [1 1 1 0], which satisfies the truth table of NAND gate.

A general logic of D Flip-Flop is developed (Fig-5) using

the logic of NAND Gate, discussed above. Five NAND gates are used where one NAND gate with dual input acts as a NOT gate .ForNAND1 and NAND3 gates, Pump and Probe pulses are selected. Outputs of NAND1 and NAND4 act as inputs for NAND2 and NAND5 respectively. By proper selection of pump and probe pulses D Flip –Flop can be realized.

The design of D Flip Flop with SOAs is shown above. Development of NAND Gate is done with the help of SOAs. Further output is observed at each end of SOA that can be tested and verified with the help of waveform.

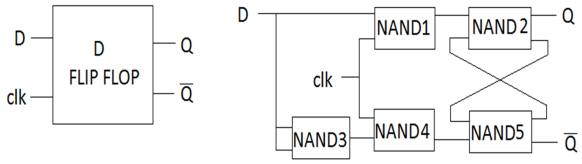


Fig 5. *Design of D flip flop.*

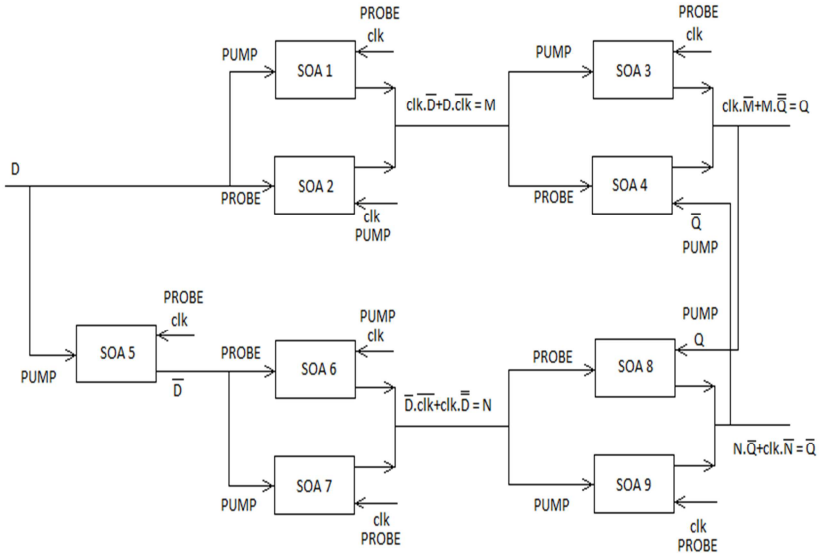
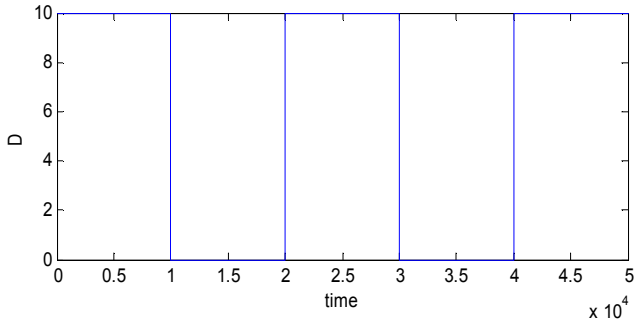
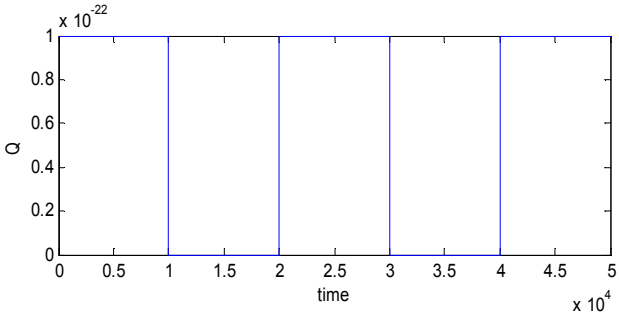


Fig 6. *Design of D flip flop using 9 SOAs.*

In Fig-6 Connection between SOA1 and SOA2 explains circuit of NAND1. SOA3, SOA4 explains NAND2. SOA5 represents the one input NAND3. NAND4 can be represented as combination of SOA6 and SOA7. SOA8 and SOA9 are used to represent NAND5.Proper labeling is done in Fig 6 to explain the different inputs used for simulation. Results are verified with the help of waveform of fig 7, which results from simulation. When D is taken as active high the output (Q) is active high. And when D is active low the output (Q) is active low. If we take the input D=[1 0 1 0 1] as shown in fig 7(a) then the output Q=[0 1 0 1] as in Fig 7(b).This verifies one output of Flip Flop. The other output can be verified similarly.



(a)



(b)

Fig 7. *(a) Input of D flip flop (b) Output of D flip flop.*

Now to make 3 bit up counter logic we need three such Flip Flops. As we have seen that a Flip Flop circuit requires 9 SOAs. Hence 3 bit up counter logic requires total 27 SOAs. The outputs of each flip flops is connected as shown in figure below.

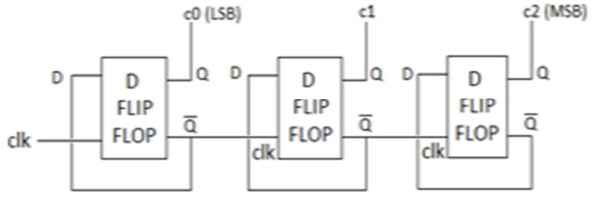


Fig 8. *3-bit up counter design.*

As shown in Fig 8, the complement output in every Flip Flop is the input itself and the clock input of next Flip Flop. External clock is given to the first flip flop. The output Q of the first flip flop is the LSB (c0) of output and the output of last flip flop is MSB (c2). When connected as discussed above, results in a 3 bit up counter logic, which can be verified with the help of waveform shown below.

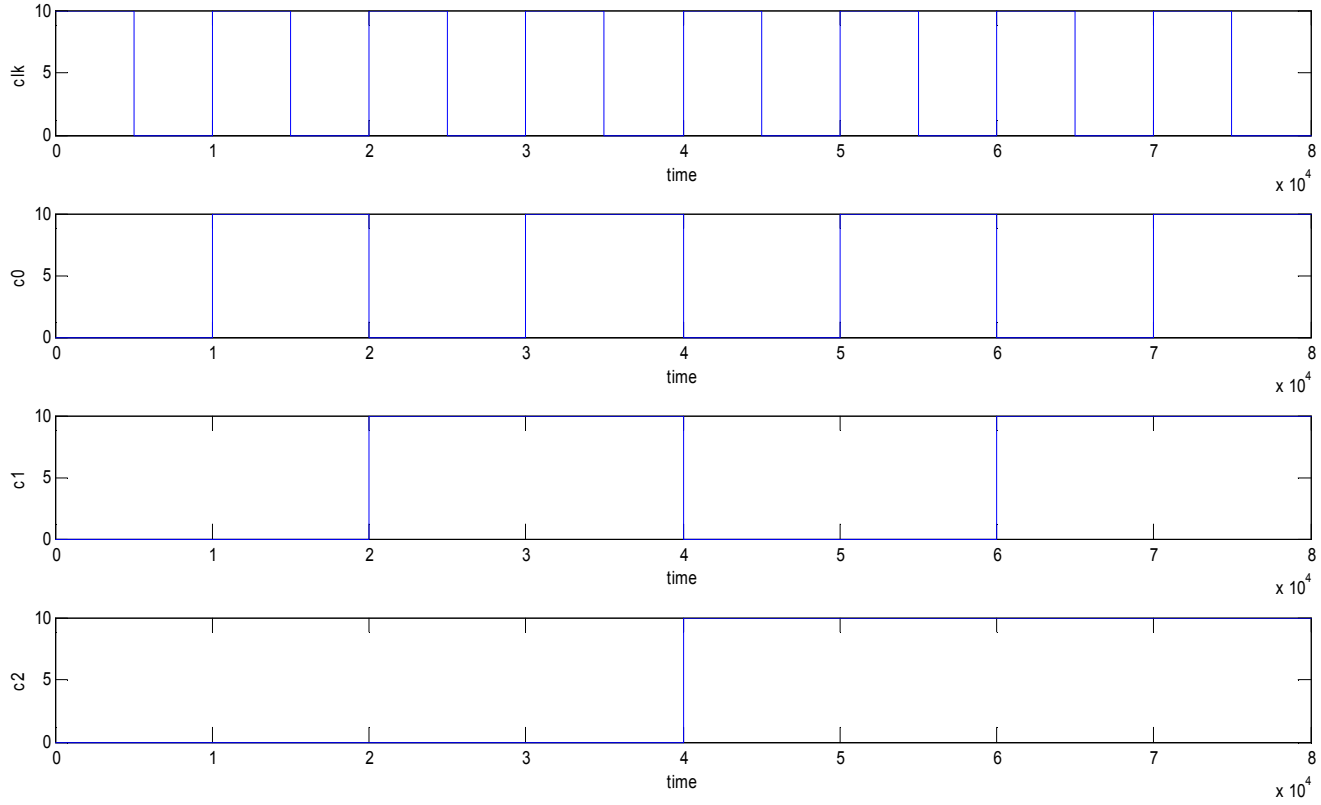


Fig 9. *Waveforms for 3 bit up counter.*

The output of 3 bit up counter namely [c2 c1 c0] starts at [0 0 0] and after every clock pulse it is incremented by [0 0 1] and after 7 clock pulses the output becomes [1 1 1]. If we give one more clock pulse to the counter then the output becomes [0 0 0]. Thus the output of 3 bit up counter is verified.

4. Conclusions

By using analytical solutions of nonlinear effects in InGaAsP semiconductor optical amplifier, we have shown that with high input pump power generated conjugate pulses can be utilized to generate different digital logic.

Based on these logics, the operation of all optical Universal NAND gate and D Flip Flop is verified and a3 bit up counteris proposed.

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